Wide field imaging spectrometer for ESA's future X-ray mission: XEUS

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Abstract

An active pixel sensor (APS) based on the DEpleted P-channel junction Field Effect Transistor (DEPFET) concept will be described as a potential wide field imager for ESA's high resolution, high throughput mission: 'X-ray Evolving Universe Spectroscopy' (XEUS). It comprises a parallel multichannel readout, low noise at high speed readout, backside illumination and a fill factor of 100% over the whole field of view. The depleted thickness will be 500 microns. These design parameters match the scientific requirements of the mission. The fabrication techniques of the DEPFET arrays are related to the high resistivity process of the X-ray pn-CCDs.

Potential extensions of the already realized DEPFET structures are a non-destructive repetitive readout of the signal charges. This concept will be presented.

As an alternative solution, frame store pn-CCDs are considered having the same format and pixel sizes as the proposed DEPFET arrays. Their development is a low risk, straightforward continuation of the XMM devices.

Potential extensions of the already realized DEPFET structures are a non-destructive repetitive readout of the signal charges. This concept will be presented.

1. Introduction

From the instrumentation point of view of large imaging spectrometers, the XEUS wide field X-ray camera is quite different from the actual XMM, ABRIXAS and AXAF focal plane instruments: The bandwidth of physical parameters is largely extended: In the final configuration the collecting area will be about 200 times larger than one. XMM mirror module. Thus readout speed must be increased and simultaneously the position resolution must be improved by a factor of 2 in both dimensions, while the total sensitive area may increase by more than a factor of 4 in the final configuration. Of course, all those changes should not affect the Fano limited energy resolution of the silicon detectors. The prospected bandwidth of the wide field imager ranges from 0.1 to 30 keV.

We introduce a development perspective for silicon X-ray detectors as a wide field imager for XEUS, based on the proven technology of high-speed fully depleted backside illuminated pn-CCDs. This focal instrument with high spatial resolution and "moderate"[1] spectroscopic resolution (as compared with gratings or cryogenic detectors) is supposed to be complementary to the cryogenic resolution (1 eV @ 1 keV), but with a small field of view.

Table 1
Physical parameters of the XMM mirror and detector system, required properties for the wide field optics on XEUS and required properties of the focal plane detectors

Characteristics	XEUS	XMM
Energy bandwidth	0.1–30 keV	0.1–15 keV
Focal length	50 m	7.5 m
Angular resolution	1–2 arcsec	15 arcsec
Req. position res. in FP:	50 μm/arcsec	10 μm/arcsec
Req. counting rate per HEW	up to 200 cps, XEUS phase A	10 cps per HEW
Req. counting rater per HEW	up to 1000 cps, XEUS phase B	
Field of view:	$\geq$ 5–10 arcmin	30 arcmin
Focal plane size:	7×7 cm^2, 14×14 cm^2	6×6 cm^2
Sensitive thickness:	500 μm	300 μm
Collect. area @ 1 keV	(5, Phase A) 30 m^2	0.15 m^2 per mirror mod.
Collect. area @ 8 keV	(3, Phase A) 3 m^2	0.05 m^2 per mirror mod.
Det. op. temperature:	180 K or higher	130–180 K
Number of res. elements:	$\geq$ 2000 $\times$ 2000	400 $\times$ 400
Detector efficiency:	90% @ CK$_\alpha$ 90% @ keV	80% @ CK$_\alpha$ 90% @ 10 keV
Full frame time res.:	$\leq$ 5 ms	70 ms
Energy resolution:	125eV@6keV	130 eV @ 6 keV
Mission life time:	25 years	10 years

The focal length of the telescope system is expected to be 50 m, the angular resolution around 1–2 arcsec (see Table 1). This translates in a required position resolution in the focal plane of 50 μm (or better), if we assume, that the spatial oversampling of 5 per dimension is reasonable. The expected collecting area at 1 keV is 5 m^2 in the first phase of the mission and 30 m^2 after the telescope upgrade. The sensitive detector area with a 10 arcmin field of view is supposed to be in the order of 14×14 cm^2.[2] The other parameters of the X-ray detector should, of course, not fall behind the state of the art of today. That is a detection efficiency above 90% between 277 eV (C$_{k_\alpha}$) and 10.98 eV (Ge$_{k_\beta}$), sufficient radiation hardness and spatially homogeneous field of view, and, if technically possible a fill factor of 100% over the whole sensitive area. The operational temperature should be comparable to the XMM operation temperature ($-90°$C) or higher. Some key characteristics of the telescope and a comparison to XMM as well as the relevant required detector properties are given in Table 1.

Two different device concepts to fulfil the requirements listed in Table 1 are considered: The active pixel sensor (1) and a frame store pn CCD system (2):

1. A new pixel detector with a position resolution of better than 40 μm, having a pixel size between 50 and 80 μm based on the DEpleted P-channel Field Effect Transistor (DEPFET) concept [1–3].
2. A frame store pn-CCD system with a position resolution of better than 40 μm, having a pixel size between 50 and 80 μm, fabricated on a high-purity silicon wafer.

Taking into account the previously introduced boundary conditions, the following performance limits should be studied for the trade-offs of the optimization strategy:

1. *The physical limits*:

- time resolution, count rate and pile-up (*highest priority*),
- energy resolution (*medium priority*),
- position resolution, adequate pixel size (*medium priority*).

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[2] If 1 arcsec corresponds to 250 μm in the focal plane with a focal length of 50 m, then 10×10 arcmin correspond to a field of view of 15×15 cm^2.

2. *The technological limits given by*:

- quality of the starting material, purity (*high priority*),
- quality of the process technology, homogeneity (*high priority*),
- monolythic focal plane coverage (*medium priority*).

3. *The operational limits, such as*:

- minimizing power consumption (*low priority*),
- high operation temperatures (*high priority*),
- radiation damage (*low priority*).

2. Technical challenges

As in all CCD-type concepts, charges are transferred slowly over large distances, they are intrinsically sensitive to radiation damage or to metallic contamination of the base material, because of the creation of traps in the bulk silicon. In addition, because of the relatively slow charge transfer, X-rays may hit the CCD during the readout time. This gives rise to events whose position cannot be reconstructed – the so-called *out-of-time* events. With the high collecting area and the good angular resolution of the XEUS mirror system, the XMM-EPIC pn-CCD systems would be limited with pile-up at count rates in the order of 10 counts per HEW and second.[3] The assumed pixel size for this estimation was $100 \times 100 \, \mu m^2$ and only 1 hit was allowed in an area of 7×7 pixels. But with the anticipated collecting area up to 30 m² several hundreds of counts per HEW and second are expected for comparable observations. That means that a factor of 20 or more in the XEUS phase A and a factor of about 150 in phase B in frame speed is needed as compared to the pn-CCD camera on EPIC-XMM, to exploit the capabilities of the XEUS mirror system.

The proposed modified pn-CCD frame store CCD system could comply with about 200 counts

per HEW according to the above pile-up definition. In dedicated read-out modes the count rate capability could be much higher by constraining the area to be read out. For the first phase of the XEUS mission with 6 m² of collecting area this count rate capability would be appropriate.

For the second phase of the XEUS project (phase B) with the final mirror size of 30 m² a second device concept has to be studied: The DEPFET active pixel detector, where every pixel is a complete single-detector sub-unit; i.e. detector and amplifying electronics in one. The readout concept of the DEPFET allows for flexible windowing on the detector during the readout. Up to 1000 full frames per second can be processed and therefore overcome most of the constraints inherent to CCDs.

The DEPFET detector is in an early development stage. Prototypes have been fabricated and proven all functional principles. While for the DEPFET arrays basic device physics research is still needed, the pn-CCD frame store concept mainly requires technological research. The pn-CCD detector is already available in a full frame mode concept and with pixel sizes adapted to the XMM optics. More details are given in Table 3.

For both concepts the problems of interconnections must be solved in a sound way: As the spacing between the readout channels shrinks by a factor of two, wedge bonding does not seem to be fully adequate. In a parallel study, we will try bump bonding techniques and wafer bonding techniques. Some preliminary tests on bump bonding techniques have already been carried out in collaboration with other institutes.

2.1. A DEPMOS or DEPFET pixel detector system with a position resolution of 40 μm or better

The DEPFET detector system belongs to the family of "active pixel sensors" (APS). That means, that every pixel has its own amplifier and can be addressed individually by external means. This results in a high degree of operational freedom and performance advantages.

1. Operation with high spectroscopic resolution at temperatures as high as $-50°C$, keeping the total readout noise at 5 electrons (rms).

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[3] Note that the pile-up limit is given by the product of pixel area and readout time per pixel. This is correct as long as the signal charge cloud is significantly smaller than the pixel size.

2. The charge does not need to be transferred parallel to the wafer surface over long distances. That makes the devices very radiation hard, because trapping, the major reason for degrading the charge transfer efficiency, is avoided.

3. The ratio between photon integration time and read out time can easily be made as large as 1.000:1, that means that the so-called out-of-time event are suppressed to a large extent.

4. As the integration time per event will be in the order of 1 ms and the read out time per line about 1 μs, more than 1000 counts per second per HEW (7 × 7 pixel) can be detected with a pile-up below 1%.

5. No additional frame store area is needed; the device is as large as the processed area.

6. Any kind of windowing and sparse readout can be applied easily, different operation modes can be realized simultaneously.

7. The DEPFET transistor amplifier structure offers the possibility for a non-destructive readout (NDR). Under those conditions the readout noise can be reduced to below 1 electron (rms) by a repetitive reading of the physically same signal charge.

From the conceptional point of view this is the most advanced semiconductor X-ray pixel detector as it offers a lot of additional features like the analog storage of 2D X-ray images. Some more recent experimental results are given in Refs [4,5]. Some conceptual system aspects and operating conditions are given in Ref. [6].

The standard DEPFET and DEPMOS devices are p-channel devices on n-type material. The use of p-type base material is very interesting for the DEPFET devices. The reasons for that is, that the use of n-channel JFETs and MOSFETs becomes possible by using holes as the signal charges. This offers an increased transconductance g_m of the transistors by a factor of three improving the equivalent noise charge at least by a factor of 1.5.

DEPFET principle

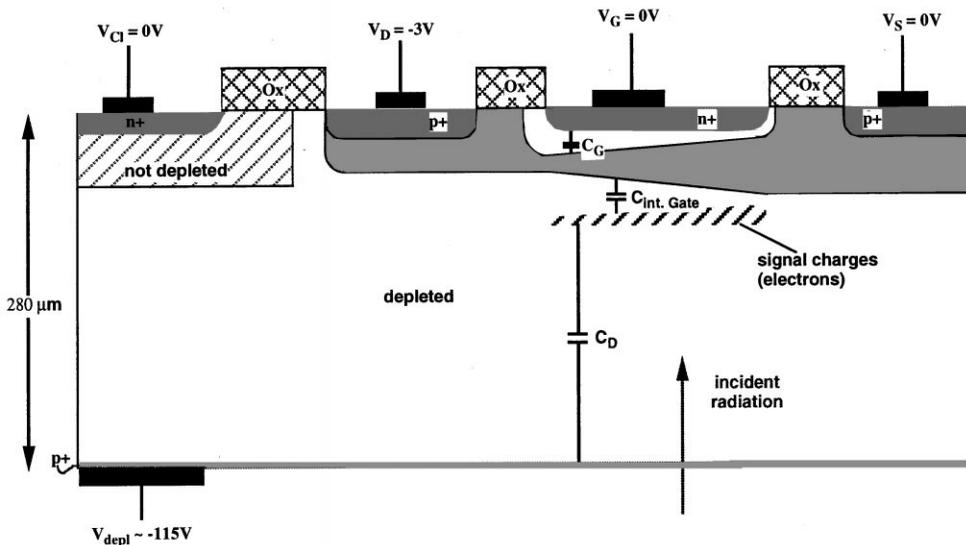### DEPFET = Field Effect Transistor operated on a fully depleted bulk

Fig. 1. Cross section of a DEPFET structure with periodic reset mechanism.

2.2. Device concept and functional principle

Our concepts are based on a detector–amplifier structure, also called Depleted Field Effect Transistor (DEPFET), which consists of a field effect transistor working on a depleted substrate. The cross section of such a device is shown in Fig. 1. The device, which was proposed by lutz and Kemmer [1], makes use of the sideward depletion principle [7]. Assuming in the following that n-type semiconductor material is used, one can deplete a detector chip in such a way, that there is a potential minimum for electrons under the channel of a field effect transistor [2]. It is straightforward to use such a device as detector, where signal charges (electrons) are collected in the potential minimum, from where they can steer the transistor current, acting as a so-called "internal gate". The result is a simultaneous integration of the first amplifier stage on the detector chip with a detection fill factor of 1.

The potential distribution in the device, calculated by the 2D TOSCA code, is shown in Fig. 2.

The potential maximum of the internal gate (minimum for electrons) is clearly visible and is separated from the external gate by the p-channel. The potential difference in the pixel area to its direct surroundings is about 1 V, sufficient to collect more than 100 000 electrons in one pixel.

Since the electrons are collected in a potential minimum – signal and leakage current, the device has to be reset from time to time by emptying the corresponding internal gate. One straightforward way of doing it, is applying a positive voltage to an adjacent n^+ contact, which acts as a drain for electrons.

In a first approach devices were built, where periodically (hundreds of μs) all charges are removed from the potential minimum beneath the transistor. This is done by applying for a short time (hundreds of ns) a positive voltage at the substrate contact. The result of a two-dimensional simulation shows the continuous rise of the bulk potential between the region under the transistor and the substrate contact for this particular case (see Fig. 3).
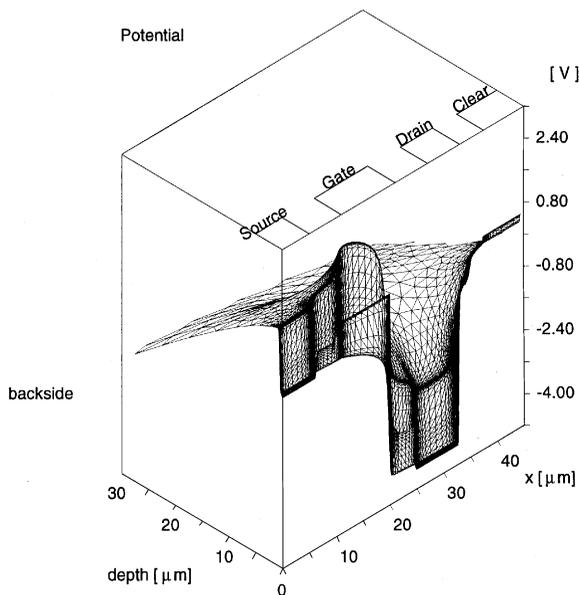

Fig. 2. Two-dimensional simulation showing the potential minimum, also called internal gate, in which electrons generated in the bulk are collected. The simulation was done with the program TOSCA for a DEPFET with cylindrical symmetry where the source is in the centre of the structure; the reader is looking from the top of the device into the bulk.
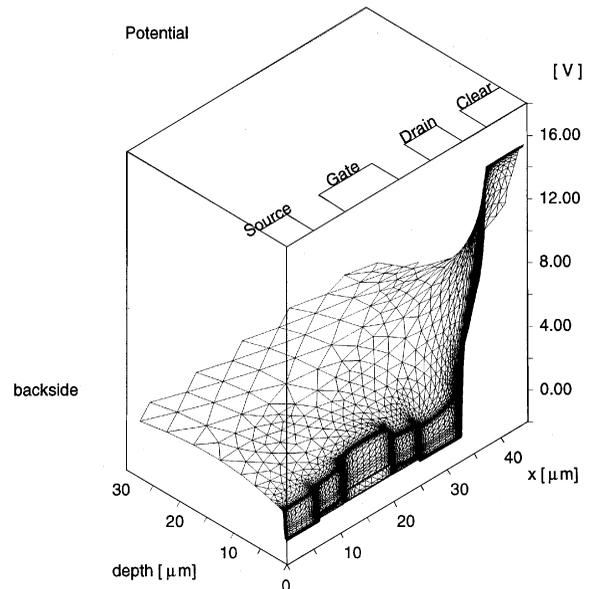

Fig. 3. Result of a two-dimensional simulation of the clear procedure; one can see the potential inside the detector chip while there is a positive voltage pulse (+ 15 V) applied to the substrate contact; the simulation was done with the program TOSCA for a DEPFET with cylindricial symmetry where the source is in the centre of the structure; the reader is looking from the top of the device into the bulk.

After the clear procedure, signal electrons can be collected and stored in the potential minimum under the transistor channel. From there they can influence the transistor current by producing image charges inside the channel, acting as if there was an "internal gate" under the transistor channel. The information about the amount of signal charges stored can be recorded by measuring the rise of the transistor current. This measurement does not disturb the stored charges, therefore the readout process can be repeated several times and opens the option of a multiple non-destructive readout. As the signal charges have to be removed explicitly and as the internal gate is continuously filled up with thermally generated electrons, the clear procedure can to be applied upon request.

2.3. Noise behaviour

Considering the noise behaviour, the so-called "detector capacitance" present in conventional detector–amplifier combinations can be neglected. As all calculations of the noise are referred to the internal gate, also any stray capacitances of the
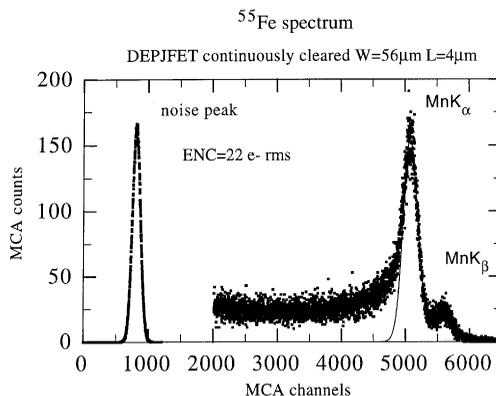
Fig. 4. Manganese spectrum measured with a DEPFET structure at 30°C with a continuous clear of the signal charges.

external gate are of no importance. This leads to very low equivalent noise charges for the series noise contribution. The parallel noise of the structure has its origin in the volume generation of charges inside the fully depleted substrate and surface generated currents. As there is a low resistance between source and gate, the gate leakage current normally can be neglected.
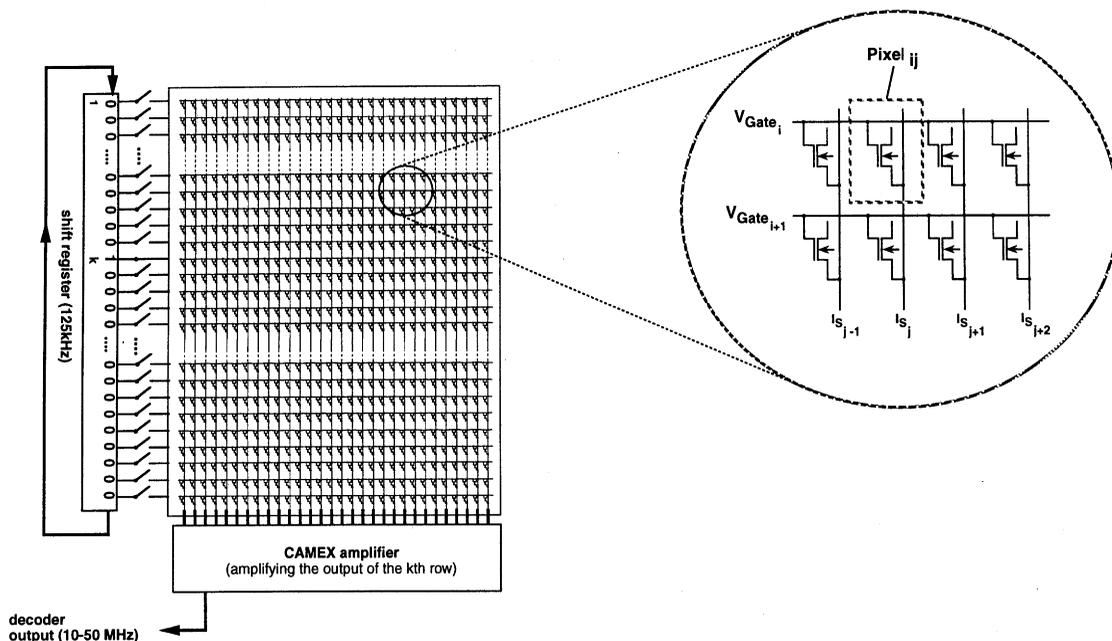
Fig. 5. Concept of the DEPFET/DEPMOS readout. Three electrical functions must be implemented: (a) amplification of the analog signals (b) control logic for the row selection and (c) the fast clear of a row. At least two different ASICS (a) and (b + c) are needed with different electrical requirements.

To examine the noise characteristics, measurements of the energy resolution were done with the help of an ^{55}Fe source. Fig. 4 shows a spectrum – recorded at room temperature – with the Mn-K$_\alpha$ and then Mn-K$_\beta$- line at 5898 and 6498 eV.

At first an energy calibration is done by comparing the position of the Mn-K$_\alpha$ line with the position of the noise peak. Afterwards the radioactive source is removed and the FWHM of the noise peak is measured.

The lowest noise figure at room temperature (20°C) of ENC = 13e$^-$ is obtained at a shaping time of 5 μs. Fitting the shaping time-dependent equivalent noise charge

$$\text{ENC}^2 = \text{ENC}^2_{\text{therm}} + \text{ENC}^2_{1/f} + \text{ENC}^{\text{leakagecurrent}}$$
$$= a_{\text{th}}/\tau_{\text{shap}} + a_{1/f} + a_{\text{leakagecurrent}} \cdot \tau_{\text{shap}} \qquad (1)$$

gives the relationship among all three major noise contributions: The series, the parallel and the $1/f$ noise. With an optimized technology (i.e. gate length 4 μm and width about 60 μm) we can obtain an equivalent noise charge around 15 e$^-$ rms at room temperature and 3 e$^-$ rms at − 50°C.

2.4. DEPFET system

The DEPFET or DEPMOS system needs essentially three electronic control and signal processing chips:

1. A control logic for the selection of the line addresses
2. A control logic for the application of the clear pulses.
3. An analog multichannel amplifier/multiplexer array for charge or current amplification of one complete DEPFET line

The basic idea of the front-end electronics is shown in Fig. 5. The control logic for the row selection and the clear can be implemented in one ASIC. In a first attempt we will fabricate prototype DEPFET devices with a pixel size of 75×75 μm^2, having a format of 128×128 pixels. This leads to a detector area of 9.6×9.6 mm^2, with a position resolution of better than 40 μm in the single photon counting mode. As already shown earlier [6] the device will be operated in a "pulsed clear mode"

with a parallel readout of the 128 channels. That means, that after each reading of one line all DEPFETs of that line will be reset with the help of an external clear pulse to bring the system back in the optimum operating conditions. The parallel (CMOS) amplifiers could be either current amplifiers or source follower configurations comparable to the parallel readout of the pn-CCDs [8].

Table 2 summarizes some of the expected properties of the proposed DEPFET active pixel

Table 2
Expected performance figures of the DEPFET focal plane detector system

Integration + Readout	
Total read time	1 ms
Integration: read time	1000 : 1
Window Mode	70 μs for 64×64 pixels
Response to radiation	
QE @ 272 eV (CK$_\alpha$)	90%
QE @ 525 eV (OK$_\alpha$)	95%
QE @ 1.740 eV (Si K$_\alpha$)	100%
QE @ 6490 eV (Mn K$_\beta$)	100%
QE @ 8050 eV (Cu K$_\alpha$)	100%
QE @ 10.000 eV	96%
QE @ 20.000 eV	45%
Depletion depth	500 μm
Partial ev. at 525 eV	5%
MIP response	150 keV
Rejection efficiency of MIPs	100%
Spectroscopy	
Fano noise at 5.9 keV	118 eV FWHM
CAMEX64B noise	2.5–3e$^-$
System noise	5e$^-$ (rms)
System noise with NDR	$\approx$ 1 e$^-$ (rms) for $n = 16$
^{55}Fe resolution	125 eV
CK$_\alpha$ resolution	50 eV
Radiation hardness	
No change up to (@260 K)	5×10^{10} p per cm^2
Focal plane geometries	
Device size	7.5×7.5 cm^2
Device format	1000×1000
Pixel size	75×75 μm^2
Position resolution	30 μm
Cosmetic defects	0.1%
Fill Factor of Focal Plane	1
Space between detectors	0%
Operating temperature	260 K

detector. The estimated properties have been derived from preliminary test results.

2.5. The non-destructive readout (NDR)

Because the electrons are confined in the electric field below the sensing gate of the DEPFET amplifier (floating gate amplifier) (Fig. 6) and are not mixed with other charges the measurement of the amount of signal charges can be repeated many times. The noise as shown in Eq. (1) can be reduced by

$$\text{ENC}(n) = \text{ENC}_o \times \sqrt{n} \qquad (2)$$

where n is the number of readings of the signal charges and ENC_o the noise of a single reading. We expect a single read noise of the DEPFET structure of $4e^-$ at $-50°C$ with a shaping time of 2 μs. Repeating that procedure 16 times, spending 32 μs for the reading of two pixels we could achieve a single-electron noise floor, corresponding to an energy resolution of less than 10 eV (FWHM). This would allow to expand the usable X-ray bandwidth down to 50 eV. As the areas which make use of the non-destructive readout can be selected during operation, we can imagine to run the detector slowly in areas where sources have been detected and fast (without NDR) where it is not required.

3. A pn-CCD system with a position resolution of 40 μm or better

The most straightforward approach towards an X-ray pixel detector with at least 3.000 × 3.000 res-olution points is a pn-CCD [9–13], an extension of the EPIC/XMM pn-CCD camera. This system was analysed in detail over the last years and a careful extrapolation of the expected parameters can be made on a broad experimental basis. The good properties of the XMM-type devices can be maintained to a large extent (high efficiency, high speed, good spectroscopic performance, high radiation tolerance, homogeneous response to radiation and so on, see also Table 3). An enlargement of the device size by a factor of two (in area) is required and a shrinking in pixel size by a factor of two per dimension is needed to get the required spatial resolution of better than 50 μm.

3.1. Basic concept

The pn-CCD detector system has been designed for the European X-Ray Multi Mirror satellite mission (XMM) (Fig. 7) which is planned to be launched in early 2000. The basic concept and layout of the detector as well as measured results are found in Ref. [1,2]. Fig. 8 shows the layout of the focal plane. The sensitive area of the detector consists of a 6×6 cm^2 large array of 12pn-CCD units monolithically integrated on a 4 in. wafer (see also Fig. 7. resistivity n-type silicon and is being read out in 4.5 ms per subunit, i.e. 75 ms for a complete cycle comprising integration and readout time. Fig. 9 gives a schematic cross section through the pn-CCD along a transfer channel. In Fig. 10, a schematic functional element of the 36 cm^2 large sensor close to the readout area is shown. The pixel
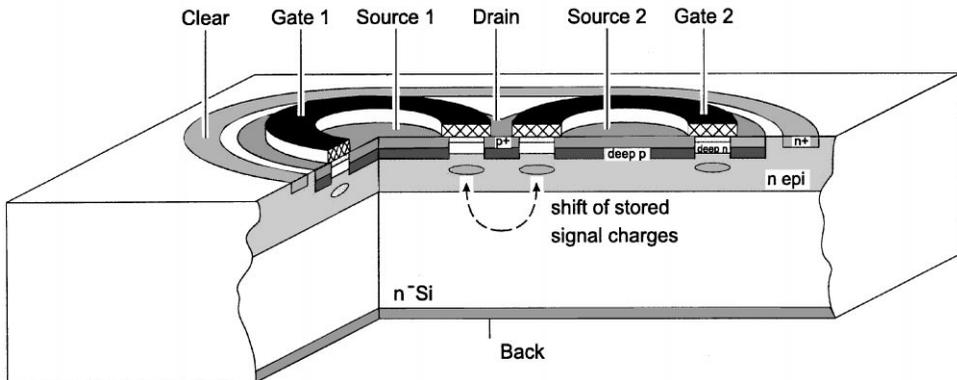

Fig. 6. Two adjacent DEPFET devices are able to transfer the signal charges from one floating gate amplifier to the neighbouring one, reading the same signal charges several times. The read noise is reduced by the square root of n, where n is the number of readings.

Table 3
Measured performance figures of the EPIC-XMM pn-CCD camera system

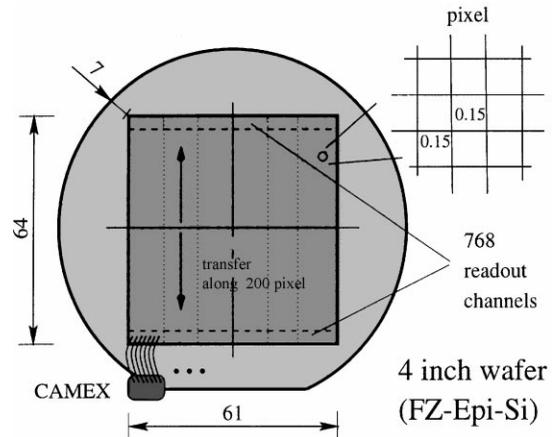| Integration + Readout	
Total read time	5 ms
Integration: read time	14 : 1
Full frame	70 ms
Window Mode	2–11 ms
Timing mode	40 µs
Response to radiation	
QE @ 272 eV (CK$_\alpha$)	85%
QE @ 525 eV (OK$_\alpha$)	95%
QE @ 1.740 eV (Si K$_\alpha$)	100%
QE @ 6490 eV (Mn K$_\beta$)	100%
QE @ 8050 eV (Cu K$_\alpha$)	97%
QE @ 10.000 eV	90%
QE @ 15.000 eV	52%
Depletion depth	300 µm
Partial ev. at 525 eV	5%
MIP response	80 keV
Rejection efficiency of MIPs	100%
Spectroscopy	
Fano noise at 5.9 KeV	118 eV FWHM
CAMEX64B noise	2.5–3 e$^-$
System noise	4.5 e$^-$ (rms)
^{55}Fe resolution	130 eV
C K$_\alpha$ resolution	70 eV
X-ray CTI (1-CTE)	1×10^{-4}
Focal plane geometries	
Device size	6×6 cm^2
Device format	400×384
Split events	$\leqslant 25\%$
Pixel size	150×150 µm^2
Position resolution	125 µm, i.e. 3.4 arcsec
Cosmetic defects	$\leqslant 0.05\%$
Fill factor of focal plane	1
Coverage of the focal plane	97%
Coverage of the focal plane	185 K
Operating temperature	
Radiation hardness	
No change up to (@175 K)	5×10^8 p/cm^2

Fig. 7. Format filling pn-CCD array on a 4 in wafer as developed for the EPIC-XMM instrument. Seven hundred and sixty eight readout channels allow for a readout time of 4.5 ms of each subunit, resulting in a total cycle time of 75 ms.

It is illuminated from the rear side, formed by an ultrathin reverse biased pn-junction. The single electrons are drifting within about 1 ns in a small cloud towards the transfer channel about 15 µm below the register surface. As shown in Fig. 10 each transfer channel is terminated by an anode and an integrated first amplifying stage which consists of a single-sided gate n-channel JFET. From there the 64 signals of each row are fed in parallel to the CAMEX64B chip [1] for amplification, shaping, sampling and multiplexing. The CAMEX output is sent to a 12-bit 10 MHz ADC. The pn-CCD camera has a size of 36 cm^2, with 150×150 µm^2 pixel size and a format of 400×384 pixels on 295 µm fully depleted high resistivity n-type silicon and is being read out in 75 ms (integration and readout).

3.2. Performance parameter

Extended measurements have been performed at the X-ray test facilities of the Max-Planck-Institut für extraterrestrische Physik. Some relevant measurement results reflecting the state of the art of the chip quality and recent improvements are briefly summarized. All measurements have been made in a single photon counting mode, except the quantum efficiency in the visible spectrum and the DC measurement at the synchrotron. All measurements
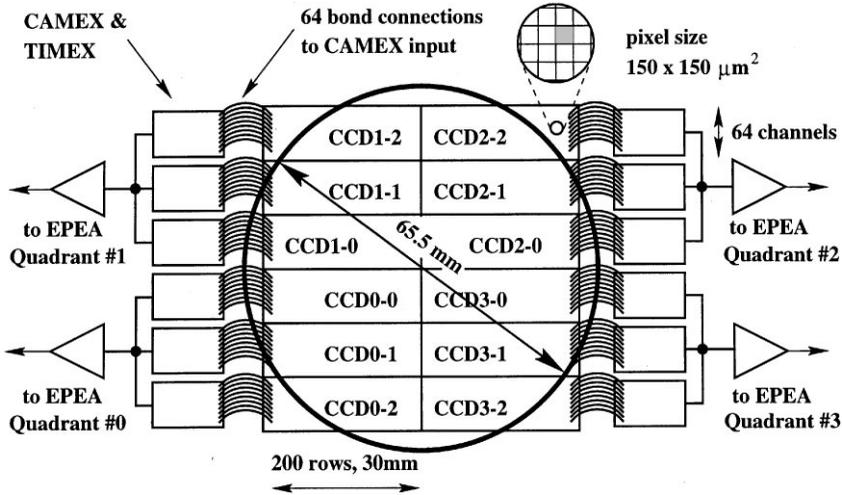
size of 150×150 µm^2 is matched to the angular resolution of the XMM telescope, which yields a half-energy width (HEW) of about 500 µm (corresponding to 15 arsec). The pn-CCD is a fully depleted silicon radiation detector [3] which is sensitive over the whole wafer thickness of 300 µm.

Fig. 8. The pn-CCD focal plane area as designed for XMM. It has a sensitive area of 36 cm², a total of 768 readout channels, multiplexed with a JFET/CMOS amplifier array at 5 MHz.
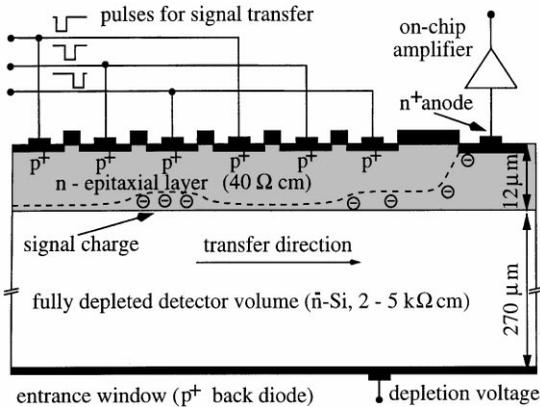

Fig. 9. A schematic cross section through the pn-CCD along a transfer channel. The device is back illuminated.

were performed at temperatures between 140 and 210 K, except the measurement of the UV, visible and infrared light.

3.2.1. Electronic and system noise, dark current

The equivalent noise charge of the pn-CCD system is 4–5 e⁻ rms for a total read cycle (integration time and readout time of 70 ms) and an equivalent pixel read time of 350 ns. The noise shows negligible temperature dependence between 120 and 190 K. The dark current contribution is small despite a sensitive thickness of 300 μm. The largest noise contribution still arises from the on-chip JFETs noise, cross talk and electronic pick-up. The readout speed is not limited by the electronic noise or transfer properties, but only by the total power dissipation of the focal plane, which should not exceed 1 W. The energy resolution at 6 keV is 140 eV at an operating temperature of 160 K. At 1.5 keV the energy resolution is around 90 eV FWHM.

3.2.2. Quantum efficiency

The quantum efficiency of our pn-type detectors – and the following remarks are equally true for the DEPFET and DEPMOS devices as well – are given by

1. the rectifying p^+n^- diode on the backside of detectors, i.e. the radiation entrance window and
2. by the depleted volume of the detector, i.e. in our case the wafer thickness.

The detectors are sensitive from the near infrared (1150 nm) up to X-ray energies of 30 keV (0.3 Å). In the IR the thickness is responsible for the good QE up to the band-gap energy of silicon of 1.1 eV, see Fig. 11. In the visible the absorption depth is in the order of microns. Around 5–10 eV, in the UV
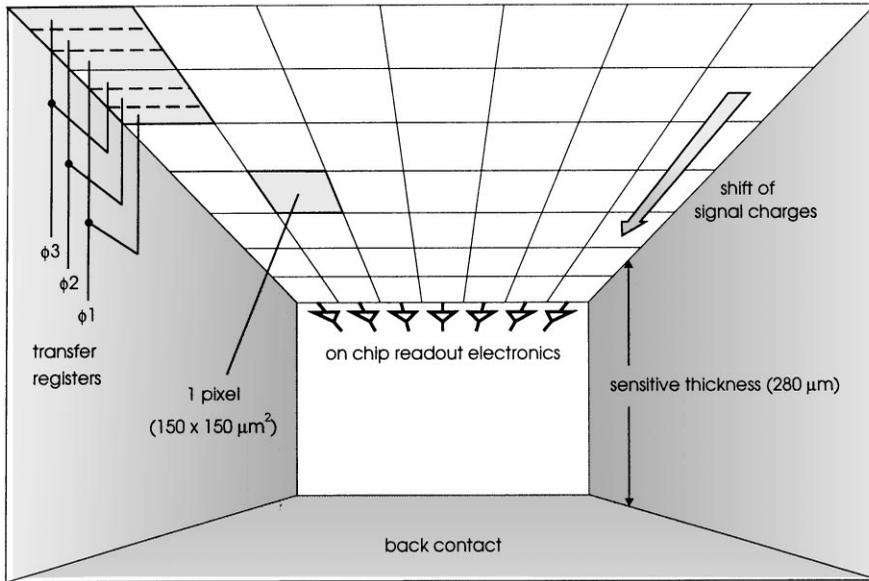
Fig. 10. Seeing the pn-CCD from the inside: The X-rays hit the CCD from the back side. Signal charges are drifted to the front side having the pixel structure due to the strong vertical electrical field. The electrons are transferred with the help of the parallel register towards the end of the column where all columns are terminated by one individual amplifier.
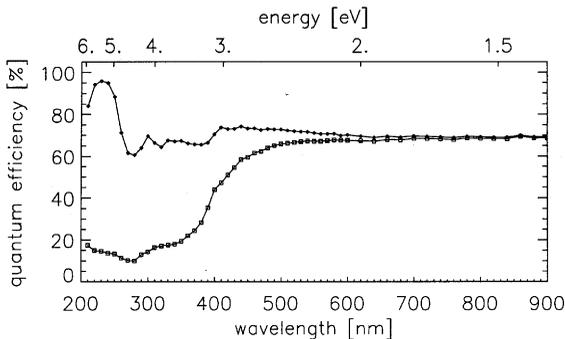

Fig. 11. Sensitivity of pn-CCDs from the UV light to the infrared light at 900 nm. The increase at 4.5 eV is due to the creation of two electron/hole pairs by one photon. The upper curve shows the quantum efficiency of the improved entrance window, the lower curve the QE of our standard entrance windows.

range, the absorption drops by three orders of magnitude to about 5 nm. For energies above 10 keV the absorption length rises up to 400 μm for energies around 30 keV over the whole bandwidth of the instrument.

Fig. 12 shows the quantum efficiency on the low-energy side of the spectrum. For X-rays in the range of 0.1 keV up to 30 keV the response is shown in Fig. 12. It is remarkable, that the change of absorption depth in silicon over five orders of magnitude is reduced to a quantum efficiency variation of less than 30% in the detectors.

3.2.3. Spatial uniformity

The spatial uniformity in the CCDs electrical performance is excellent. The recent fabrications created a large number of wafers with homogenous noise distribution and uniform spectroscopic behaviour. Only a small number of single defects (about 0.1 defect per cm^2) occurred. In the PANTER test facility, where the X-ray source is located 130 m far from the pn-CCD, a flat field illumination was made with $Ti_{L\alpha}$ ($E = 452$ eV). The spatial homogeneity of the response was better than 1%. The measurement precision was limited by the statistics. Operated in a single-photon counting mode each individual pixel was exposed to approximately 20 photons. The photon rate per readout frame was lower than 100 per cm^2, the frame rate was 14 per second.
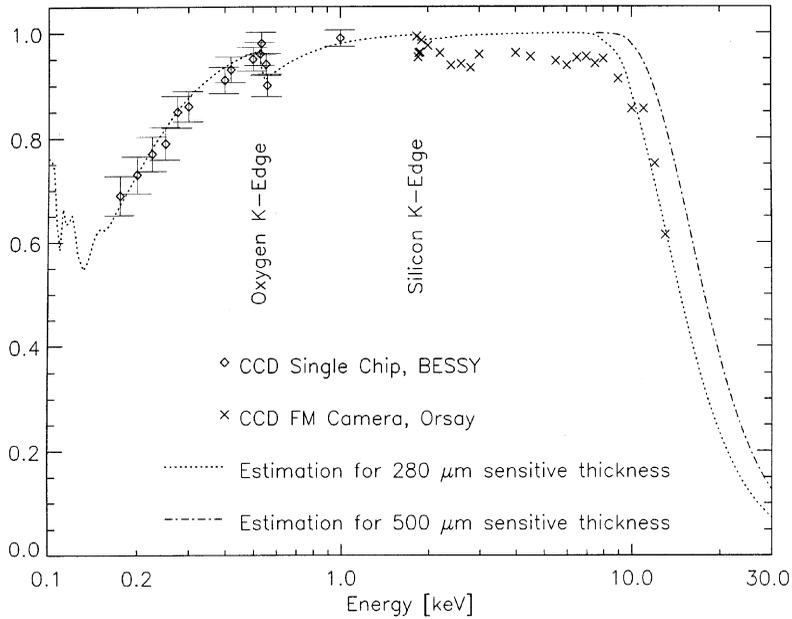
Fig. 12. Quantum efficiency measured in a DC photocurrent mode (solid line) and in a single photon counting mode (+ signs). The dotted line is the QE calculated from the photon absorption coefficients. The calculated detectivity for a 500 μm thick detector shows 40% QE at 20 keV.

Fig. 13. Example for a pn-CCD operated in a frame store mode. The imaging area has a pixel size of $75 \times 75 \ \mu m^2$ and the store area of $50 \times 50 \ \mu m^2$.

3.3. PN-CCD frame store CCDs for XEUS

As in conventional CCDs pn-CCDs equally can be designed in a frame store format. The area to be processed in a quasi-defect-free manner increases by the size of the store area. A $7 \times 7 \ cm^2$ large image area can be realized monolythically on a 6 in wafer (see Fig. 13). If pn-CCDs should be used also for the $14 \times 14 \ cm^2$ focal plane a possible extension of the focal plane camera is shown in Fig. 14. By that technique the whole field of view could be covered with a minimum of insensitive gaps in between the buttoned devices. The central part, the inner diameter of 7 cm, would be homogeneously sensitive.

The major change in concept besides the smaller pixel size is the dramatic increase in frame rate because of the modified readout philosophy: By doubling the processed area and dividing it in an image and store section we will get the required readout speed for the large collecting area of the XEUS mirrors. As will be shown later, we except to get a frame rate of the whole camera of 200 per second. That lead us to a count rate capability of
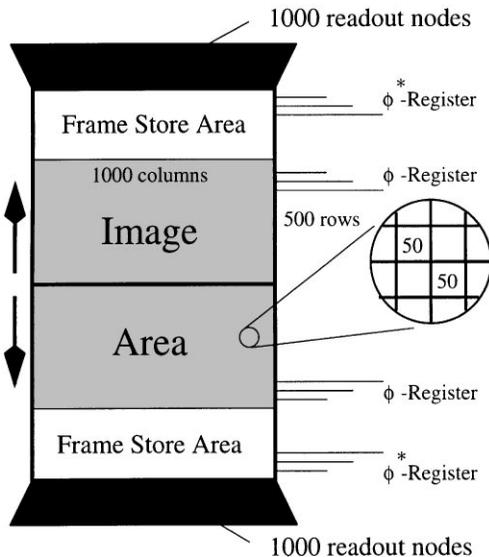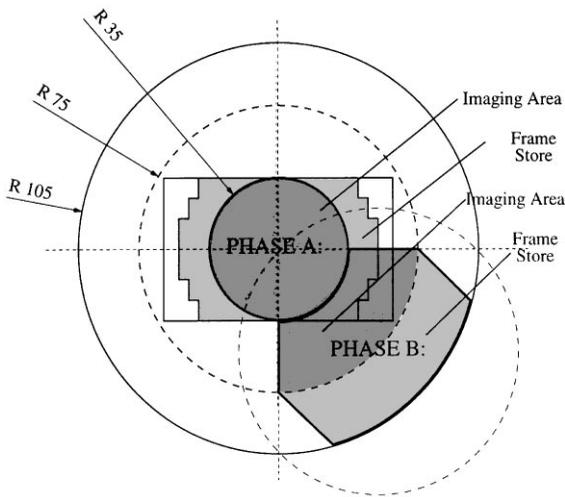
Fig. 14. Composittion of the whole focal plane with frame store pn-CCDs. The outer CCDs are slightly cylindrically shaped.

more than 200 counts per second and half-energy width.

As the pixel size shrinks, the number of read nodes and transfers increases. At the same time, the system will be requiring more read-out time and being more sensitive to radiation damage due to the higher number of transfers. If charge sharing of signal charges among more than one pixel is needed for the improvement of position resolution, the effective read noise per event will be higher by a factor $\sqrt{n}$ (n is the number of pixels involved). To maintain the high readout speed of the pn-CCD EPIC-XMM system, the signal processing must be speeded up by a factor of two. The solution of the above "constraints" seems to be realistic, but must be proven experimentally.

To date, the signals of one row (64 pixels) are processed in parallel in 22 μs. The extension to 128 channels on the CAMEX amplifiers, to match the new pixel pitch, was already realized for applications in high-energy physics, but it would involve a redesign of the CAMEX64B for the low noise operation. In addition the signal process time must be shortened by a factor of two. The increased read out speed will certainly have an impact on the power consumption which is actually below 1 W for the 36 cm^2 array.

If 128 channels are read out with 12.8 MHz, 10 μs would be required for the parallel readout of

one pixel line. For the parallel transfer from the image to the storage area 100 ns are needed for one transfer. A device of 1000×1000 pixels would be divided (as in the XMM-EPIC case) in two identical halves of the image area, i.e. 500×1000 pixels each. For the parallel 500 shifts 50 μs would be needed for the transfer from the image to the insensitive storage area. The readout for the storage area while integrating X-rays in the image part, would then be $500 \times 10\ \mu s = 5$ ms. That means, within 5 ms the whole focal plane would be read out. The out-of-time probability for the X-ray events will then be 100:1. In this operation mode 200 image frames can be taken in 1 s with a full frame time resolution of 5 ms.

According to our present knowledge learned from the fabrications of the pn-CCD for EPIC-XMM, two different pixel sizes for the "pn-CCD solution" are proposed.

1. Pixel size $50 \times 50\ \mu m^2$ (storage area)

- high resistivity n-type Silicon on 6 inch wafers, sensitive thickness: 300–500 μm

2. Pixel size $75 \times 75\ \mu m^2$ (imaging area)

- high resistivity n-type Silicon on 6 inch wafers, sensitive thickness 300-500 μm, modified channel stop to optimize the spreading of the charge cloud for optimum center of charge finding.

On one side the higher thickness of the fully depleted 6 inch silicon wafer helps to avoid mechanical problems of handling. But physically that offers a larger lateral diffusion of the signal charges, thus improving the position resolution and it increases the detection efficiency to 40% at 20 keV. The prototype devices, available in the beginning of next year, will have formats of up to 128×128 pixels, that corresponds to a sensitive area up to 1×1 cm^2. The challenge for the realization of this *extended* frame store pn-CCD is mainly in the technological domain.

4. Pixel size and position resolution of devices on high resistivity silicon

Due to the diffusion of the signal charges during their drift from the conversion point inside the
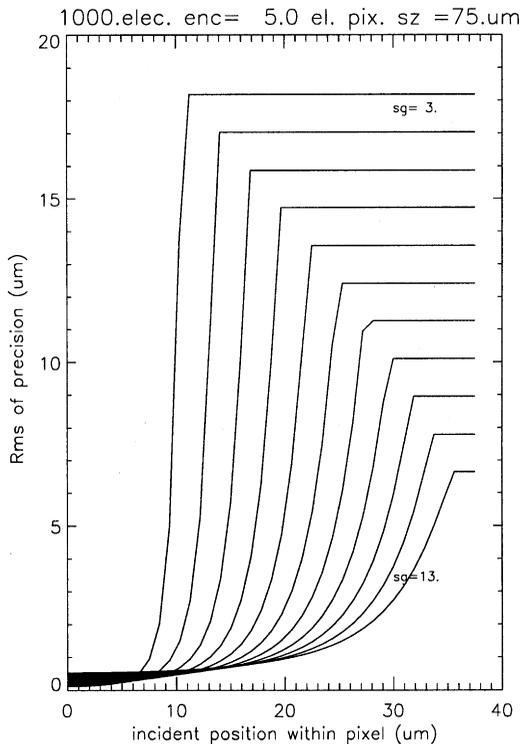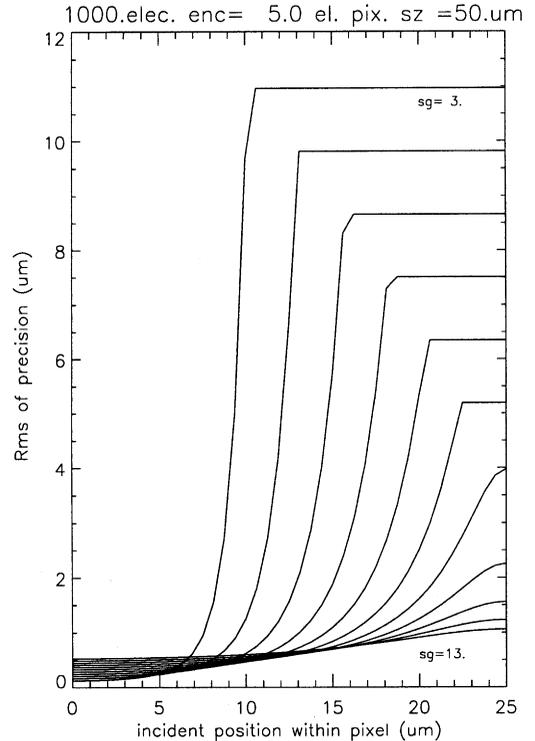
Fig. 15. Improvement of the position precision as a function of the gaussian spreading of the electron charge cloud. The typical sigma of the gaussian ("sg") electron distribution is 7 μm. The assumed pixel size is 75 μm.

Fig. 16. Improvement of the position precision as a function of the gaussian spreading of the electron charge cloud. The typical sigma of the gaussian ("sg") electron distribution is 7 μm. The assumed pixel size is 50 μm.

silicon into the potential minimum of the pixel, the position resolution can be improved substantially, with relatively large pixel sizes. The improvement is significant, if the signal charge cloud diameter is in the order of the pixel size. Taking into account the thicker silicon wafer (6 in version) and the longer transit times, i.e. collection times for the generated electrons, the charge cloud, containing 97% (4 σ) of all signal charges will have a diameter of about 30 μm. This would improve the spatial resolution with a pixel size of 50 μm to less than 15 μm for the events which are all contained in one single pixel (less than 20% of all events) and to a spatial resolution substantially below that (≤ 5 μm) for all other events (80%) (see also Fig. 16). For the needs of that mission that leaves sufficiently safety margin with respect to the number of the desired resolution points.

In the case of a pixel size of 75 μm about 70% of all events will be split events and 30% are con-

tained within one pixel. Under those conditions, the position resolution will be always better than 40 μm, but for most of the cases better than 20 μm (see also Fig. 15). Those values may be changed by (a) the temperature, (b) by the pixel layout and (c) by the operating voltages.

A theoretical and experimental study on the position resolution using the charge spreading technique and their impact on energy resolution must be considered.

Figs. 15 and 16 demonstrate the effect of charge spreading and position reconstruction of the incident photon.[4] The X-axis indicates the position of the photon hit: At 0, the photon hits the pixel exactly at the boundary to the neighbouring pixel.

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[4] The improvement of the position resolution because of the extension of the electron charge cloud is equally true for the DEPFET detector.

Here the position resolution is at this optimum. As the physical situation is symmetrical with respect to the centre of the pixel, the X-axis ends at half the pixel size. On the ordinate we plotted the position resolution (rms). This number must be multiplied by a factor of three, if the position of more than 90% of the photons is better than the rms value on the ordinate. As a parameter "sg" (sigma of the Gaussian) is plotted the (rms) lateral signal spread before arriving in the pixel well. The upper curve indicates a sg = 3 μm and increases to sg = 13 μm at the bottom. For a 500 μm thick detector the typical "sg" is between 7 and 9 μm.

5. Conclusions

A new wide field imager is proposed, able to match the scientific requirements of the XEUS mission: The energy resolution will be Fano limited, the quantum efficiency nicely covers the bandwidth from 0.1 keV up to 30 keV and the readout is fast enough to handle more than 1000 counts per second within the point spread function of the X-ray telescope with a pile-up below %.

The potential of the further development of fully depleted pn-CCDs indicates the use of the devices up to 200 full frames per second, maintaining all imaging and spectroscopic properties.

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