Novel pixel detectors for X-ray astronomy and other applications

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Abstract

Following previous work in particle physics, the MPI Semiconductor Laboratory has been founded with the purpose of developing novel semiconductor detectors for particle physics and X-ray astronomy. A short description of the already successfully concluded development of pn-CCDs for focal imaging in X-ray astronomy (XMM/Newton X-ray Observatory) is given and the much more demanding requirements in a future X-ray astronomy experiment (XEUS) are discussed. A new type of pixel detector is proposed which will be capable to meet these requirements. It is based on the "DEPleted-Field Effect Transistor (DEPFET)" principle. The device operated on a fully depleted silicon wafer allows an internal charge amplification directly above the position where the signal conversion takes place. A very low gate capacitance of the DEPMOS transistor leads to low noise amplification. In contrast to CCDs, neither transfer loss nor "out-of-time events" can occur in a DEPFET-array. A very interesting feature is the possibility of repeated non-destructive readout which can be used for noise reduction even for the low-frequency ($1/f$) noise. This type of detector will also have its applications in linear collider experiments.

1. Introduction

The development of semiconductor detectors for nuclear radiation detectors originated in particle physics and was later transferred to other fields of science. Of particular interest is the application in X-ray astronomy, where silicon CCDs have been introduced as focal instruments of space-based X-ray mirror telescopes in the recently launched CHANDRA and XMM/NEWTON [1] satellite missions. In contrast to previously used gas detectors, these semiconductor detectors provide good energy resolution in addition to the excellent position measurement. One of these telescopes is equipped with a pn-CCD, a device based on a novel device structure and shows excellent device properties. Based on previous experience from introduction of semiconductor detectors into particle physics, this device has been developed over a period of 12 years at our institutes. It was the main driving force for setting up our semiconductor laboratory in which these detectors were produced.

In this paper we give a short description of the laboratory, the XMM/Newton mission with the pn-CCD and discuss the requirements in a future proposed X-ray mission (XEUS). Order(s) of

magnitude increase in readout speed and improved radiation hardness are required.

Based on a new principle we have developed the concept for a pixel detector that will meet these requirements. With modifications, this device will also be applicable to the conditions to be expected in future linear colliders as planned in particle physics (e.g. LEAR at DESY, Hamburg).

2. The MPI Semiconductor Laboratory

The MPI Semiconductor Laboratory has been founded with the aim of providing commercially not available silicon detectors for particle physics and X-ray astronomy. The complete silicon technology available in this laboratory is adapted to the special requirements of semiconductor radiation detectors. Particular important features are the ability to build wafer-size defect-free double-sided-structured detectors on ultrapure silicon.

A photograph (Fig. 1) shows part of the old cleanroom in which the detectors described in this paper have been manufactured. Later, the laboratory was moved to a new location with improved cleanroom and technology.

3. Semiconductor detectors for X-ray astronomy

CCD detectors have recently been introduced for focal imaging in space-based X-ray telescopes. The USA (NASA)-supported CHANDRA mission uses modifications of optical (MOS) CCDs.

The European XMM/NEWTON satellite [1] (Fig. 2), the most powerful X-ray telescope ever built, launched on December 10, 1999 with an Ariane 5 rocket carries three X-ray Wolter-type mirror telescopes (Fig. 3) which focus X-rays in the energy range of 100 eV–15 keV onto their focal planes. Two of those telescopes are equipped with MOS CCDs, one with our pn-CCD. The three X-ray telescopes and an optical telescope observe the same region of the sky corresponding roughly to the size of the moon.

The mirror system is a technical masterpiece [2] (Fig. 4). Each telescope contains 58 concentric mirror shells of 2 m length and 0.5–1 mm wall thickness. Extreme geometrical precision and surface roughness or few tens of atomic layers are required for shallow angle total reflection and focal resolution of 0.5 mm.

4. The pn-CCD on the XMM/Newton observatory

The pn-CCD [3,4] now operating successfully on the space-based XMM/Newton X-ray Observatory has been developed over a period of 12 years at our institutes in Munich. It was the main driving

Fig. 1. Old cleanroom of the MPI Semiconductor Laboratory.

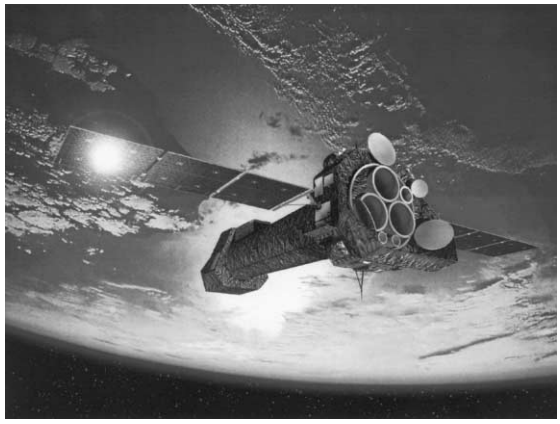

Fig. 2. Artist view of the XMM/Newton satellite with its three X-ray and one optical telescopes.

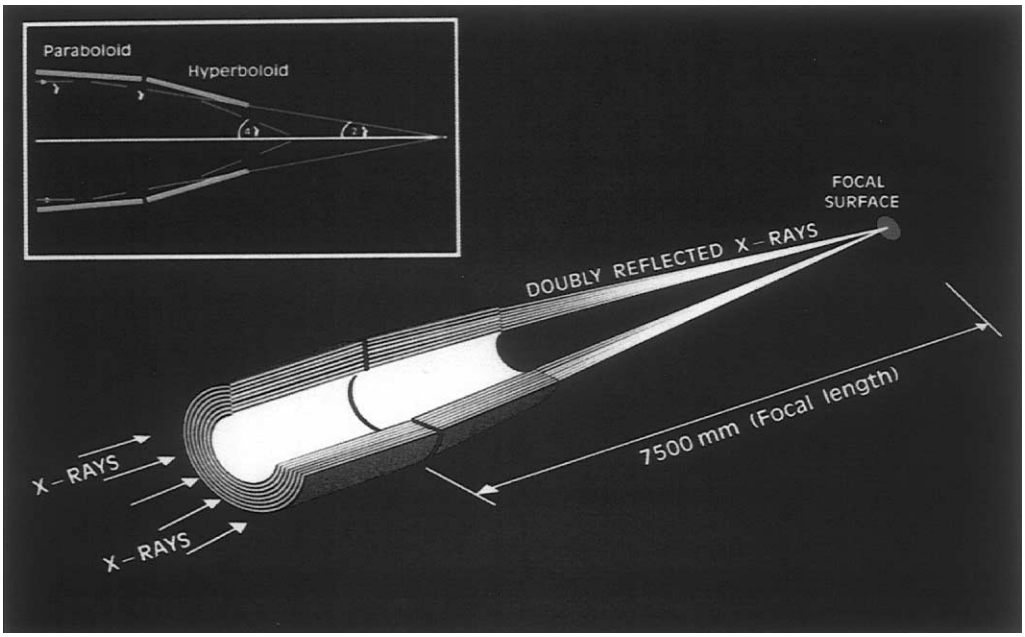

Fig. 3. The Wolter-type X-ray telescope.

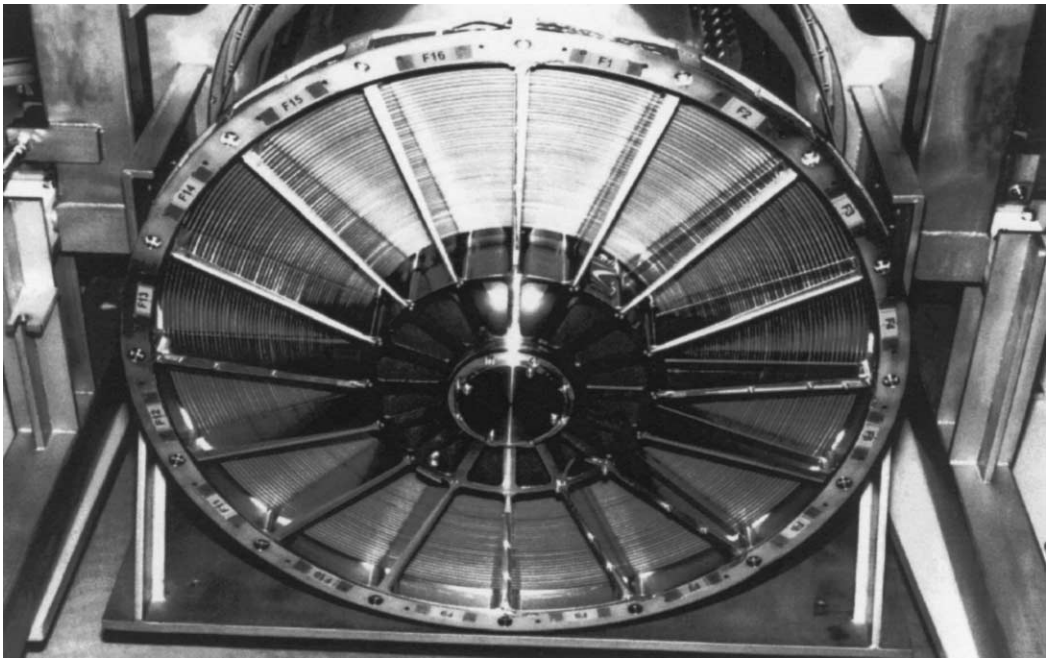

Fig. 4. The XMM mirror system consisting of 58 nested paraboloid–hyperboloid mirror shells seen from the backside.

force for the foundation of the MPI Semiconductor Laboratory in which this device was built.

The 6×6 cm^2 device (Fig. 5) operates according to a new principle which is based on the silicon drift chamber [5] and has been optimized for the forseen application. The schematics of a cut through the wafer along the channel is shown in Fig. 6. The wafer is completely depleted and, therefore, fully sensitive and the radiation enters from the lower (back) side through a uniform thin entrance window. Diode-strip transfer registers shift the collected signal charges at a depth of ≈ 10 μm to a readout node. The relatively large 150×150 μm^2 pixel size is matched to the special resolution of the telescope. Together with the readout topology (parallel readout of columns through separate readout nodes) a readout speed (4 ms for the complete device) several orders of magnitude higher than conventional CCDs is achieved.

The pn-CCD has been integrated into the X-ray camera (Fig. 7), and the satellite launched with an Ariane 5 rocket on December 10, 1999. It delivers X-ray images of the sky of excellent quality. Fig. 8 shows the first XMM X-ray image recorded at the XMM/Newton Observatory. An interesting region in the large Magellanic Cloud has been selected. The quality of this image can be appreciated only when false colors providing the information on X-ray energy are reproduced.

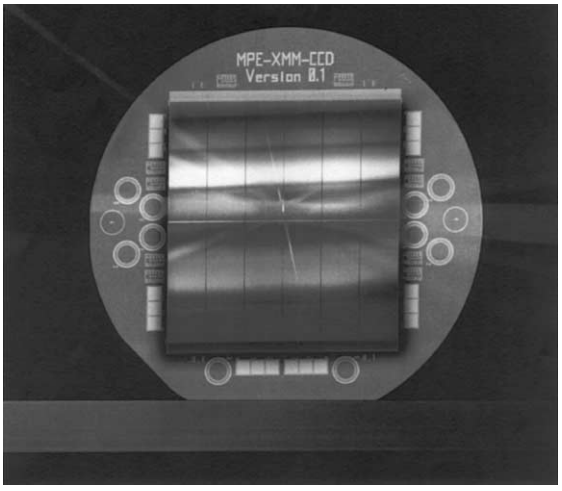

Fig. 5. Photograph of the 6×6 cm^2 pn-CCD produced on a 4 in silicon wafer at the MPI Semiconductor Laboratory.

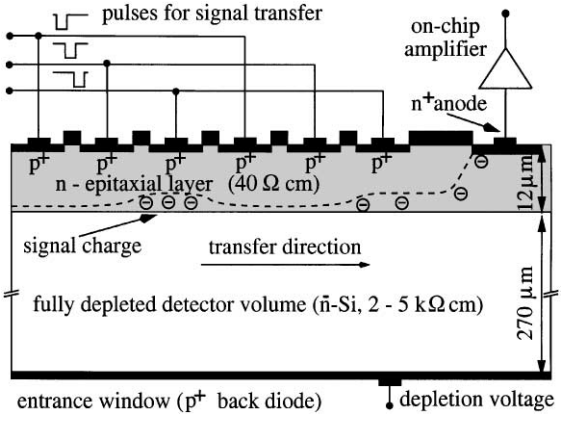

Fig. 6. Operation principle of the pn-CCD: cut along one transfer channel.

5. The proposed future X-ray mission XEUS

The proposed XEUS X-ray observatory [6] (Fig. 9) with its focal length of 50 m is too large to fit on a single satellite. Instead, two separate spacecrafts will carry mirrors and focal imaging. Even the mirror system is too large to be launched in one go. Therefore, the mirrors will be assembled

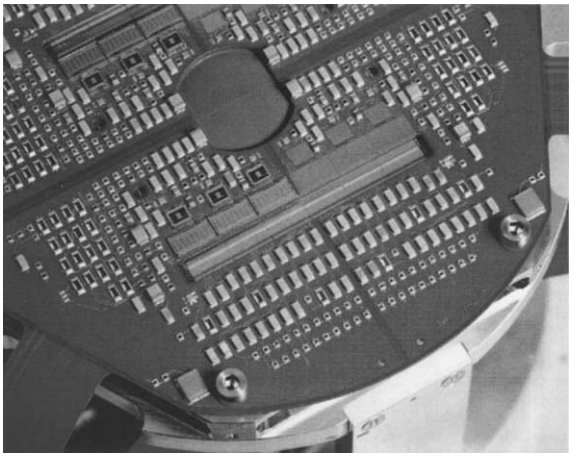

Fig. 7. The pn-camera focal plane. The pn-CCD is located below the electronics multilayer board. The radiation enters from below.

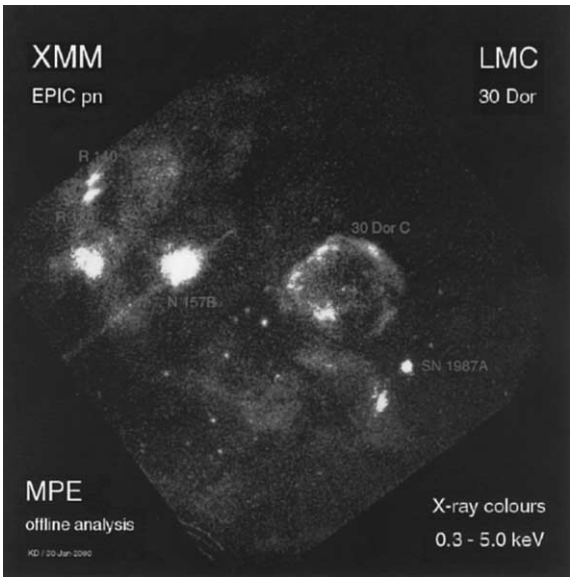

Fig. 8. The first X-ray observation with the XMM/Newton Observatory.

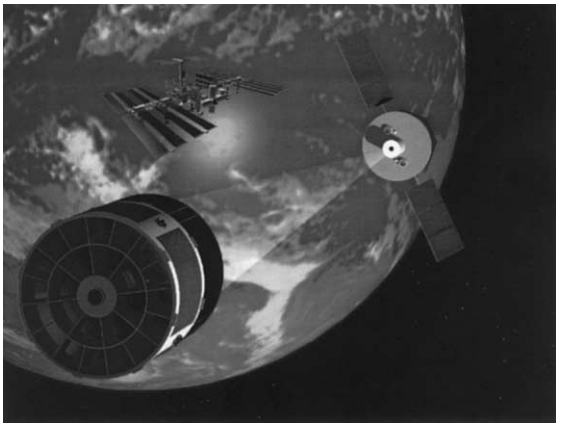

Fig. 9. An artist image of the proposed XEUS X-ray observatory.

on the international space station seen in the background of the picture.

Compared to XMM/Newton, the requirements for the focal instrument are very strongly increased (see Table 1) and can hardly be met with CCD technology (see Ref. [7] for a comparison of options for focal imaging). For this purpose, we propose, a new device which according to our understanding keeps all good properties of the pn-CCD and will be able to meet these challenges. Of particular importance are the need of much faster readout, the avoidance of "out-of-time events" which are collected in the CCD during readout and have wrong position assigned, the larger focal area and the smaller pixel size.

The new device uses the DEPFET structure which will be described in the following section.

6. The Depleted-Field Effect Transistor (DEPFET)

The DEPFET principle has been proposed in 1985 by Kemmer and Lutz [8]. It has been subsequently verified experimentally [9] confirming its interesting properties. It has been considered as an alternative to the already started development of the pn-CCD for the XMM mission. At that time, the decision went in favor of the continuation of the pn-CCD. More recently, it was considered for applications in biophysics and a development program of DEPFET pixel detectors to be applied in autoradiography was initiated and has led to good results [10,11].

6.1. Operation principle of a DEPFET

The principle of the DEPFET is shown in Fig. 10. It is based on the sideward depletion as used in the semiconductor drift chamber and the field effect transistor which can be of MOS-type (as shown in the figure) or junction type. The transistor is located on top of a low-doped n-type semiconductor substrate. It becomes fully depleted by applying a sufficiently high negative voltage to the backside $p+$ contact. By suitable doping, a potential minimum for electrons is formed below the transistor channel. The fully depleted bulk is the sensitive volume of the detector in which electron–hole pairs created by the incident radiation are separated by the electric field. While the holes are moved to the negatively biased backplane, the electrons are collected in the local potential minimum below the channel of the transistor (the "internal gate") and thus increase its charge density by induction. As a consequence, the transistor current is increased as long as the

Table 1
Comparison of focal plane requirements for XEUS and XMM/Newton

Characteristics	XEUS	XMM	Detector requirement
Energy bandwidth	0.1–20 keV	0.1–15 keV	sens. thickness: 500 μm
Focal length	50 m	7.5 m	
Angular resolution	1–2 arcsec	15 arcsec	
Position res. in FP	250 μm/arcsec	36 μm/arcsec	50–100 μm
Field of view	5–10 arcmin	30 arcmin	7×7 cm^2, 14×14 cm^2
Collect. area @ 1 keV	6–30 m^2	0.5 m^2	—
Collect. area @ 8 keV	3 m^2	0.05 m^2	—
Det. op. temperature	180 K or higher	130–180 K	180 K and higher
Number of res. elements	$\geq 1000 \times 1000$	400×400	1000×1000 or more
Detectors efficiency	90% @ C K_α 90% @ 12 keV	85% @ C K_α 90% @ 10 keV	$\geq$ 90% from 0.1 to 12 keV
Full frame time res.	1–5 ms	70 ms	1–5 ms or better
Energy resolution	125 eV–6 keV	130 ev–6 keV	50 ev–1 keV, 125 eV–6 keV

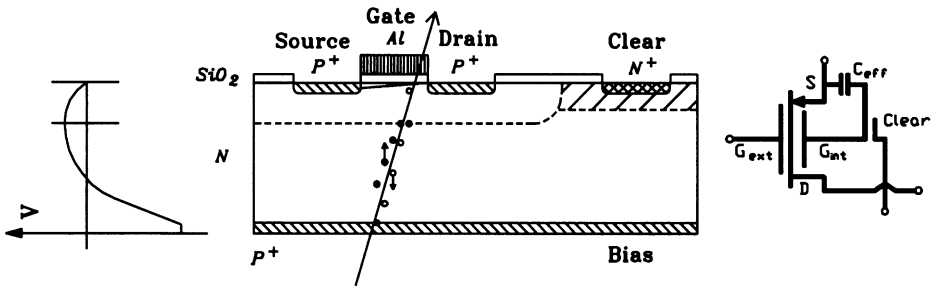

Fig. 10. The DEPFET structure and device symbol.

signal charge is not removed from the internal gate.

Removal of the charge (emptying of the internal gate) can be performed in several ways, some of them will be described below. The device symbol for the DEPFET is shown in Fig. 10. It is derived from the usual transistor symbol, adding the internal gate and the reset contact.

6.2. The use of DEPFET arrays as pixel detectors

Arranging many DEPFETs over an extended area leads to a pixel detector array with each single DEPFET providing one pixel. By choosing suitable voltages on sources, drains and gates of the transistors, one can turn on a single transistor (or a group of transistors) and measure the charge collected in the selected pixel (or group of pixels) by comparing the measured transistor current with the value obtained for empty internal gate. As the signal charge is not destroyed by the act of measurement, the signal can be measured repeatedly and also with varying granularity (by choosing different combinations of pixels). Fig. 11 shows an arrangement of DEPFETS in which each pixel (or a group of pixels) can be read out individually. In this arrangement, the drains of the DEPFETs are connected in a columnlike fashion, while sources and gates are connected in rows. Also indicated in this circuit diagram are clear electrodes which are used for emptying the internal gates. They are also connected in a row-like fashion. The methods for clearing internal gates will be discussed below.

Several schemes for readout are possible. The drain currents of each individual pixel in the row may be read out in parallel or, as indicated in the figure, in series through one output node if the

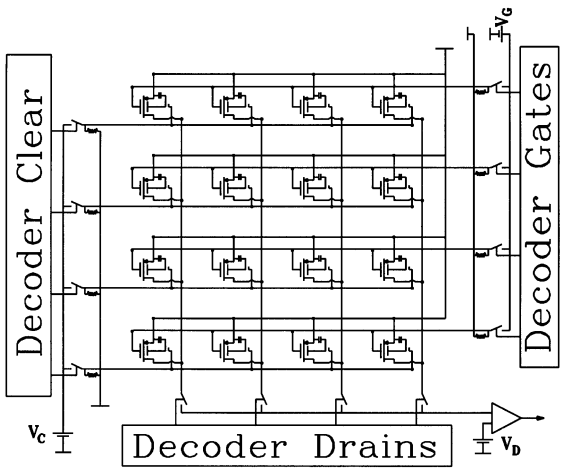

Fig. 11. The circuit diagram of a DEPFET matrix with one single output node. Parallel readout by providing each drain column with a separate readout electronics leads to a large increase of readout speed.

multiplexer for the drain current (on the bottom of the figure) is included. For applications in X-ray imaging, continuous scanning of rows and subsequent clearing seems most natural when full-frame readout is desired. Contrary to readout of CCDs, the signal charge is not moved to an output node, but is read out at the location of production. Therefore "out-of-time events" (data collected during the readout cycle of CCDs with wrongly assigned position information) are completely avoided.

Several principal points have to be addressed in order to arrive at a satisfactorily working device: clearing of the signal charge (of the internal gate); the pixel topology; the readout method and the topological layout of the matrix. These points will be discussed below. An additional proposal addresses the reduction of electronic noise in a double-DEPFET-switcher arrangement.

6.3. DEPFET topologies

Principally, one distinguishes between open and closed geometries. Open geometries are usually linear structures in which source and drain are of rectangular shape connected by the channel which is steered by the gate. For these topologies, care has to be taken to avoid detrimental effects due to the sideward limits of the structure. In closed geometries (often of cylindrical form) the source is surrounded by the gate and the drain. This way all problems connected with the sideward boundary of the transistor channel are avoided.

For DEPFETs only closed geometries of p-channel type have been pursued so far (see e.g. Refs. [9,11]). Both, MOS-enhancement and JFET-type DEPMOS transistors have been successfully operated. As the DEPFET transistors are built on detector-grade low-doped silicon, additional buried n-type doping fairly close to the surface is necessary in order to move the position of the internal gate close to the surface (at a distance smaller than the gate length) and to simultaneously prevent the flow of holes from the transistor through the bulk towards the strongly negatively biased backside diode. Closed geometries avoid the complications arising at the sideward borders of the channel, however, substantially larger chip area and channel length are required. Furthermore, the methods for clearing the internal gates are restricted.

6.4. Methods for clearing and signal measurement

After each readout the internal gate has to be emptied. Contrary to standard readout where the signal charge is added to a large sea of charge, in the DEPFET the internal gate contains only the signal (neglecting the leakage current). Complete clearing of the internal gate, therefore, avoids the noise due to fluctuations in the left-over charge. In closed geometry clearing can be performed across a potential barrier towards an n-doped clear contact embedded in the source or the drain of the transistor. In open geometries, the clear contact can be located also to the side of the channel. In the latter version, fast clearing of a geometrically small internal gate can be achieved. Common to both geometries is the necessity to prevent signal charge from reaching the clear contact instead of the internal gate during the charge collection phase. This can be accomplished by implanting a buried p-doped layer beneath the clear contact.

The signal is measured by the difference of the transistor currents, with and without signal charge being present in the internal gate. For the empty state, one can take either the measurement before the signal charge deposition or the status immediately after clearing. While the first method works also for incompletely cleared internal gate, it has disadvantages with respect to noise performance since it is sensitive to low-frequency noise. In addition, the currents have to be read out twice and the first readings stored throughout the complete readout cycle in order to be able to compute the difference, while for the second option the difference can be evaluated directly.

7. Noise reduction by multiple reading

A rather fundamental problem in noise filtering is the presence of low-frequency noise, in particular the serial component with a $1/f$ frequency characteristics which is present in almost all devices. Contrary to white (or thermal) noise, the $1/f$ signal-to-noise characteristics does not improve with signal shaping time, but remains almost independent on the type of shaping.

The possibility of shifting the signal charge out and into the internal gate – respectively, shifting it between the internal gates of two neighboring DEPFET transistors – opens up a way for multiple "independent" measurements of the same charge in order to reduce the measurement error to a very low level. With such a structure, the amplifier-generated (serial) noise decreases approximately proportional to the square root of the number of measurements, even for the $1/f$ noise component [12,13].

8. Layout and device simulations of a pixel cell

We will present one example of a pixel cell which allows the switching of charge between the internal gates of neighboring DEPFETS. This combined with repeated non-destructive readout, leads to strong noise reduction.

A perspective view of a single pixel is shown in Fig. 12. The single p-doped drain (D) is in the center of the cell. It is connected with the two sources (S1 and S2) through the MOS enhancement channels below the gates (G1 and G2). The signal charge is stored within the internal gates located below the channels. These internal gates are formed with the help of buried (deep n) n-type implants (DN). The signal charge can either be switched between the two internal gates or cleared towards the n+ clear contact (Cl) that is underlayed by a buried p-implant (DP).

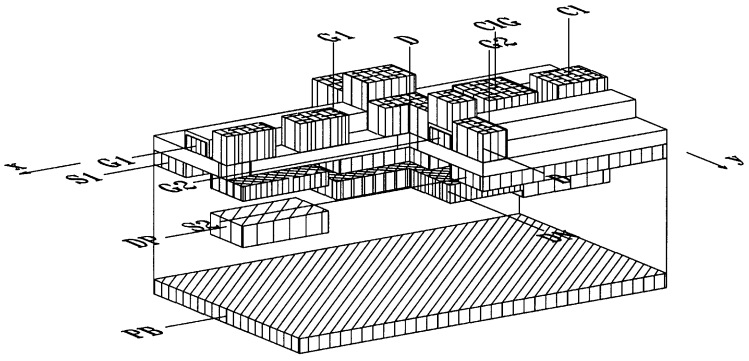

Fig. 12. The DEPFET matrix with charge switching option: perspective view of a single simplified cell. p+ doped sources (S1, S2) and Gates (G1, G2) of neighboring cells are connected in x-direction through a first connecting layer, p+ drains (D) in y-direction through the second connecting layer. The connections for n+ clear contacts (Cl) and clear gates (ClG) are not shown in the drawing. The internal gates are formed by the buried deep-n implantant (DN). Shielding of the n+ clear contact from the bulk is accomplished with the help of the buried deep-p implant (DP). The bulk is depleted from the backside with the help of the p-layer (PB) which simultaneously forms the radiation entrance window.

Two-dimensional device simulations for critical cuts through the device have been performed using the TOSCA program [14] to study the response of the device to radiation, the functioning of the clear mechanism and the transfer of charge between the two internal gates when the option of noise reduction by switching and repeated readout is used.

The response of the drain current of an already turned on DEPFET to the charge deposition caused by a 5.9 keV X-ray is shown in Fig. 13. The first narrow peak is the induced signal created in the initial phase of charge separation. The stable situation is reached after approximately 30 ns.

Clearing of the internal gate is performed by the application of a positive voltage pulse of approximately 12 V to the clear contact. Fig. 14 displays the amount of charge left in the internal gate during the clearing cycle when applying a fairly slow (rise time 10 ns) clearing pulse. All charge has disappeared after 15 ns. It has also been verified that no charge is injected when the clear contact returns to its normal state.

Finally we show in Fig. 15 the switching process, in which the charge is transfered between the internal gates of two neighboring transistors across the common drain. The top part of the figure shows the charges in the two internal gates while the time sequence of the switching signals applied to the drain and the two external gates is shown in the lower part of the same figure.

During the transfer, the drain is put at source potential (0 V) so as to reduce the potential barrier between the two internal gates. The external gate at the side from where the charge is to be moved is put at negative and the other external gate at positive potential. One notices that the charge is transfered within few nanoseconds. Within 25 ns, less than 0.1 electrons are left in the original internal gate.

These results demonstrate that the operation of the device is intrinsically very fast and that the readout and clearing speed will rather be limited by effects in the signal routing.

9. Application of DEPFET matrices in X-ray astronomy and other fields of science

In the previous section, a single DEPFET matrix concept has been described. We will discuss

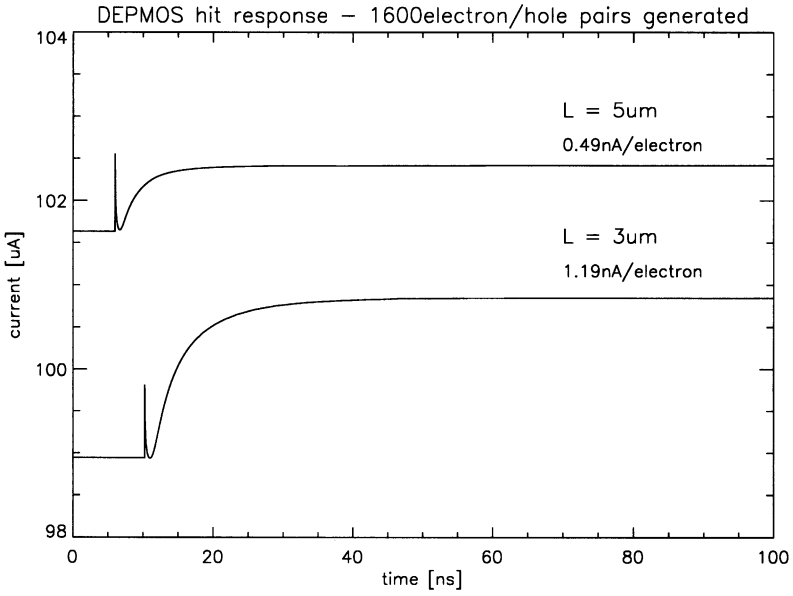

Fig. 13. Current response of the DEPFET operated at a current of about 100 μA to the charge deposition corresponding to an X-ray of 5.9 keV energy for two channel length of 5 and 3 μm.

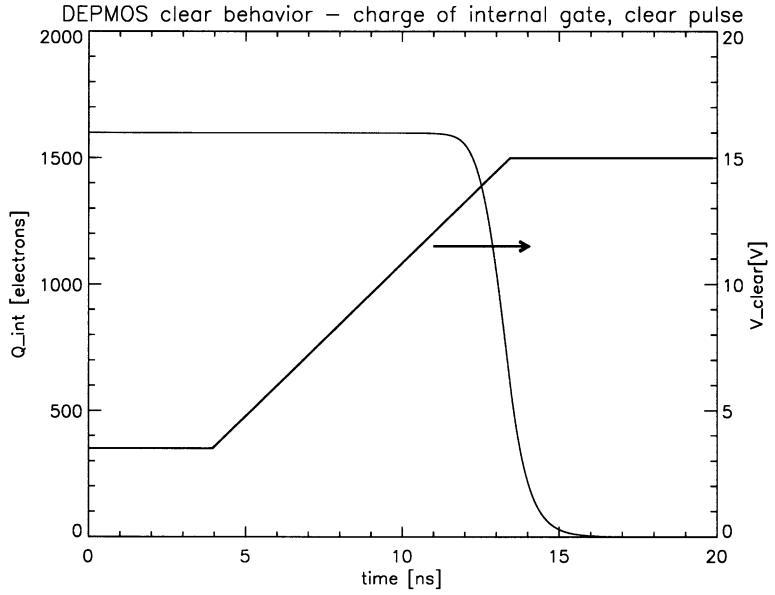

Fig. 14. Clearing of the internal gate: time dependence of the charge in the internal gate for a 15 V clear pulse with 10 ns rise time.

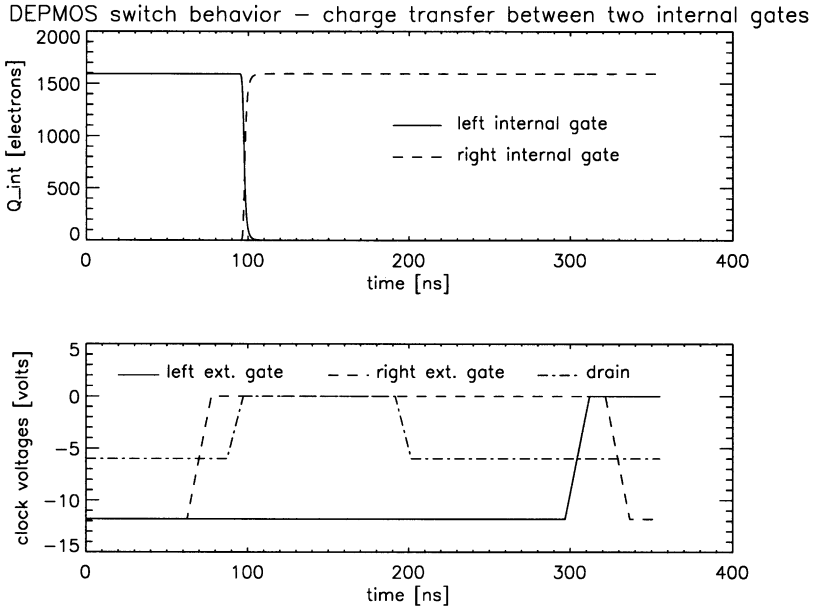

Fig. 15. Double-DEPFET structure: time dependence of the charges in the internal gates during the switching process (top) and voltages applied to external gates and common drain (bottom).

now the more general question on what is to be gained from this and other concepts. This will be done for applications in X-ray imaging, and to lesser degree also for other applications.

These pixel detectors are ideal candidates for focal imaging in X-ray telescopes. CCDs have very recently been employed for this purpose (Chandra and XMM/Newton). The proposed DEPFET

detectors, in many respects, share the good properties of the pn-CCDs [3]: sensitivity over the full wafer thickness, uniform thin radiation entrance window on the wafer side opposite to the electronics and improved radiation hardness compared to front side illuminated MOS CCDs. The latter property is due to the fact that low-energy particles entering through the mirror optics are absorbed in the detector bulk before reaching the sensitive front region (self-shielding).

Additional good properties will be obtained with the new devices. Transfer of charge across many pixels towards an output node is completely avoided. Instead, the charge is measured directly at the position of creation. Thus transfer losses, a major problem in CCDs – especially after radiation damage – are no issue. The wrong position assignment for photons collected during readout is also avoided. In order to keep these events at reasonable low value, CCDs are operated with a collection time at least an order of magnitude larger than the readout time. DEPFET matrices instead can be read out continuously row by row, each readout being followed by clearing the row.

The individual addressing of pixels (or rows of pixels) allows more sophistication in the readout. It is for example possible to read individual regions in the matrix at high rate and simultaneously others with low rate. This is useful when the amount of data to be processed has to be limited and data pileup of bright objects require high-speed readout. This option is also of interest for the observation of rapidly varying objects.

For the low-energy range, spectral resolution is limited by electronic noise. The method of switching the signal charge between two transistors provides a means to reduce this electronic noise to a negligible value. The spectral resolution is then limited by the charge-generation process (Fano noise).

The very low noise obtainable in DEPFET matrices and the possibility of measuring space points make these devices also very attractive for particle tracking in elementary particle physics experiments. Due to the excellent noise properties, detectors can be made very thin and are, therefore, well suited for measuring low-momentum tracks. However, in the described readout method, the low time resolution poses a problem. This, however, can be overcome in specific applications, as for example, at the proposed linear electron collider TESLA. Here the collisions of the pulse trains occuring within ≈ 1 ms are followed by a ≈ 200 ms gap which can be used for readout of individual pixels. Information on the time within the 1 ms collision can be provided when all transistors of the matrix are turned on during this 1 ms period and prompt signals are derived from e.g. rowlike connected transistors.

As CCDs, DEPFET matrices will also have their applications in X-ray observations apart from astronomy. Of particular interest are X-ray diffraction and spectroscopy in material science, medicine, biology and experiments on synchrotron radiation facilities.

10. Conclusion

CCD-type pixel detectors developed and produced at our laboratory have been used very successfully in X-ray astronomy. Matrix detectors based on the DEPFET structure offer very important advantages for focal imaging in X-ray astronomy and other applications when compared to presently used detectors (CCDs). These advantages are due to the intrinsic properties of the structure which at the same time has detector and amplifier properties. High amplification and low noise can be obtained and the charge can be read out at the place of origin, thereby avoiding problems connected with charge transfer. Device simulations on a prototype design confirm that the device is intrinsically fast and that it will function properly. This prototype will make use of a mechanism which shifts the signal charge repeatedly between two neighboring transistors, thereby reducing electronic noise to a very low level. The DEPFET matrix prototypes will be produced at the MPI Semiconductor Laboratory.

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References

[1] F.A. Jansen, XMM: Advancing science with the high-throughput X-ray spectroscopy mission, ESA Bulletin 100, special issue, ESA Publications Division, December 1999, pp. 9–12.
[2] B. Aschenbach, U. Briel, F. Haberl, H. Bräuninger, W. Burkert, A. Oppitz, P. Gondoin, D. Lumb, Imaging performance of the XMM-Newton X-ray telescopes, in: J. Trümper, B. Aschenbach (Eds.), Proceedings of the SPIE, Astronomical Telescopes and Instrumentation 2000, X-ray Optics, Instruments, and Missions, Munich, Paper 4012-86, 2000.
[3] L. Strüder et al., Rev. Sci. Instr. 68 (1997) 4271.
[4] P. Holl et al., Trans. Nucl. Sci. NS-45 (1998) 931.
[5] E. Gatti, P. Rehak, Nucl. Instr. and Meth. A 225 (1984) 608.
[6] R.B. Hoover, A.B.C. Walker (Eds.), The X-ray Evolving Universe Spectroscopy Mission (XEUS), SPIE, Proc. Vol. 3766 (1999) 82–159.
[7] L. Strüder et al., SPIE 3766 (1999) 127.
[8] J. Kemmer, G. Lutz, Nucl. Instr. and Meth. A 253 (1987) 365.
[9] J. Kemmer, G. Lutz et al., Nucl. Instr. and Meth. A 288 (1990) 92.
[10] P. Klein et al., A DEPFET pixel bioscope for the use in autoradiography, Nucl. Instr. and Meth. A 454 (2000) 152.
[11] P. Klein et al., First measurements on a DEPFET active pixel matrix for X-ray imaging spectroscopy, J.E. Trümper, B. Aschenbach (Eds.), SPIE Proc. Vol. 4012 (2000) 605.
[12] C. Pho Duc, Test und Weiterentwicklung eines rauscharmen Silizium Strahlungsdetektors, Diploma Thesis August 1994, Munich University, Preprint MPI-PhE/95-03.
[13] R.P. Kraft et al., Nucl. Instr. and Meth. A 361 (1995) 372.
[14] H. Gajewski et al., TOSCA – Two Dimensional Semiconductor Analysis Package, Handbuch, WIAS, Berlin, 1992.