Analysis of Background Events in Silicon Drift Detectors

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Abstract

Measurements of the energy resolution and the peak-to-background ratio of a Silicon Drift Detector at several positions and biasing voltages are performed. The origins of events with partial charge collection, which contribute to the background, are identified. A model describing the different mechanisms and the spatial distribution of partial events is developed. By optimizing the biasing voltages, an improvement of the peak-to-background ratio of up to 20% is obtained.

Key words: Silicon Drift Detector, peak-to-background ratio, partial events

1 Introduction

The Silicon Drift Detector (SDD) produced by Ketek GmbH/MPI Halbleiterlabor Munich is a compact, high resolution x-ray detector, which is commercially available since several years. It is widely used in x-ray fluorescence analysis, diffractometry, element imaging in scanning electron microscopes, and synchrotron applications. Its typical energy resolution is 140 eV (FWHM) at 5.9 keV and −15°C. This temperature is reached using an integrated thermoelectric cooler, and thus no liquid nitrogen for cooling purposes is needed.

The objective of this work is to identify the origin of events with partial charge collection, which contribute to the background, and to develop a model describing the different mechanisms and the spatial distribution of partial events. As a basis for the model, measurements with different collimator diameters and small spot sizes are performed (section 4). The whole detector is scanned several times, to determine the variation of the peak-to-background ratio and energy resolution depending on the spot position. In contrast to previous investigations by Kappen et al. [1], where a 7-element SDD was analyzed, the effects of bias voltage changes are also considered. Addi-

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tionally, the doping profiles, the electric potential, and the charge carrier distribution of the SDD are calculated (section 5). Thus, the different mechanisms of charge loss are identified.

2 The Silicon Drift Detector

The working principle of the SDD is described in many publications, such as [2,3,4], so only a brief overview is given here. The SDD is based on the principle of sideward depletion introduced by Gatti and Rehak [5]. A high resistivity semiconductor (n-type Si for this SDD) is depleted by a small n^+ ohmic substrate contact (outer substrate) with respect to the rectifying p^+ junctions, which cover both surfaces of the chip. On one surface (the upper side) of the chip, strip-like segmented p^+ junctions are biased in such a way, that an electric field parallel to the detector's surface emerges. Electrons released within the depleted volume drift within this field towards the n^+ anode. For applications in x-ray spectroscopy, a modified design was proposed by Kemmer and Lutz [6,7], with drift electrodes at only one side, and a large area pn junction at the entrance window (see fig. 1).

An n-channel JFET is embedded inside the ring-shaped anode. Electrons produced by incident radiation are lifted to the conduction band and drift to the anode. The resulting voltage change at the anode is directly coupled to the p^+ gate of the transistor by a small metal strip.

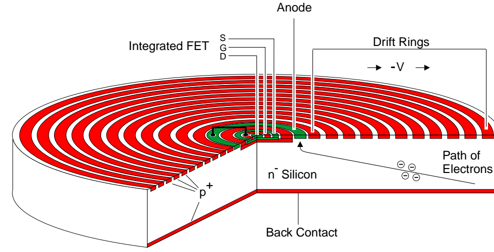

Fig. 1. Scheme of the Silicon Drift Detector. The charge generated within the depleted volume is drifted to the read-out node by an electric field, which is generated at the drift rings. The detector is illuminated from the back side.

The negative voltage on the gate reversely biases the junction. Thus, the transistor channel is depleted, resulting in drop of the current, which flows through the transistor.

The JFET is separated from the anode by a negative potential applied to the inner guard ring (IGR), which is located between the source and anode rings.

As the anode is small, the SDD's output capacitance is very low and independent of its active area. Together with a good capacitive matching between the SDD and the integrated JFET, this leads to a very low noise level and insensitivity against microphony and pickup effects. Because the rate of thermal generation of charge carriers is very low, its optimum energy resolution is already reached at about $-15°$C, and it can be even operated at room temperature. Due to its small overall capacitance, the SDD's best energy resolution is obtained at short shaping times ($\leq 1\mu$s). Thus, the SDD is particularly suited for applications at high count-rates (up to $10^6\,\mathrm{s}^{-1}$).

The peak-to-background ratio of both, $5\,\mathrm{mm}^2$ and $10\,\mathrm{mm}^2$ SDDs, is typically 500, whereas values of up to 20,000 are attained for Si(Li) detectors. For this reason, an analysis of the origin of the background is performed in the following sections, and possible improvements are proposed.

3 Definitions

The energy resolution σ_{FWHM} is defined as the full width at half maximum of the Mn K_α peak at 5.9 keV. For the definition of the peak-to-background ratio p/b, both the peak height p and the mean background b need to be defined:

p = peak height of the Gaussian fit of the Mn K_α peak (5.9 keV) without background subtracted.

The mean background b is the average number of counts in the background region $E_{\mathrm{min}} \dots E_{\mathrm{max}}$:

$$b = \frac{1}{a(E_{\mathrm{max}}) - a(E_{\mathrm{min}})} \sum_{j=a(E_{\mathrm{min}})}^{a(E_{\mathrm{max}})} n_j \quad (1)$$

n_j is the number of counts for each ADC channel j, and a is the ADC channel number of the energy bin corresponding to $E(a)$. For spectra with high statistics ($\geq 10^6$ total counts) in section 4.1, the lower end of the background region E_{min} is set to 0.8 keV, and the upper margin E_{max} to 1.2 keV. For the spot measurements with relatively low statistics in section 4.2, E_{min} is set to 1 keV and E_{max} to 3 keV. This larger background region is used in order to reduce the statistical error of p/b, as the small aperture size leads to a very low count rate, and therefore only spectra with a total of about 10^5 counts are obtained. As the background is distributed very homogeneously over the complete energy range, the p/b ratios for different E_{max} vary less than 20 %.

Because the peak height p becomes smaller for worse energy resolutions σ_{FWHM}, the peak-to-background ratio p/b decreases linearly with increasing σ_{FWHM}, as the area below the peak remains constant. To analyze the effects of partial event generation independently from the energy resolution, the variable "peak probability" ω is introduced here. It is defined as the area below the Mn K_α and Mn K_β divided by the number of all events between 0.5 and 7 keV. Thus, ω gives the probability of an event to be found within a peak, and not within the background. Due to the finite size of the SDD, a certain fraction of the events show up within the escape peak, and ω cannot become 1.

4 The measurements

All measurements are performed with a standard $5\,\mathrm{mm}^2$ SDD, fabricated at the MPI Halbleiterlabor, Munich on <100> Silicon. The SDD chip and the thermoelectric cooler are enclosed into a TO 8 housing, which is filled with N_2 at atmospheric pressure. At the radiation entrance side, an 8 μm Be foil is glued into a

Zr collimator. The collimator length is 1.8 mm and the distance between its lower end and the chip surface is 0.8 mm.

To dissipate the heat produced by the thermoelectric cooler, the SDD module is mounted to a large Cu block. The distance between the ^{55}Fe source and the surface of the chip is $\approx$ 5 cm, in order to achieve a good collimation. For the spot measurements (section 4.2), the ^{55}Fe source and the two apertures are attached to an x-y-stage, which has a precision of better than 1 μm.

4.1 Different collimator radii

At first, the peak-to-background ratios are measured for various radii r_c of the collimator, which is mounted to the housing. This results in different illuminated areas πr_i^2 from 0.5 mm^2 to 5 mm^2. In fig. 2, the p/b values for several radii of illumination r_i are shown (the corresponding collimator radii are slightly smaller). For $r_i < 1.1$ mm, p/b increases steadily with larger collimator radii. It reaches a maximum when the SDD is almost completely illuminated, except for the last drift ring (R 17). As soon as the margin of the active area gets illuminated as well, more partial events occur, and the p/b ratios become worse. An explanation of the dependence of p/b on the illuminated area is given in section 4.3.

4.2 Spot measurements

In order to localize more precisely the regions, where charge splitting begins to occur, the following measurements with a strongly collimated ^{55}Fe x-ray source are carried out.

The first spot measurement is performed with relatively large aperture sizes. Two apertures with a diameter of 200 μm are used, resulting in a spot diameter of about 300 μm (FWTM). This is done in order to roughly locate the regions with partial charge collection and to verify, if p/b is symmetric with regard to the center of the SDD (which is found to be the case). The p/b ratio is small at the center and at the margin of the active area, and very large at the intermediate region.

At these points, where neither the read-out node, nor the outer region are illuminated, very high p/b ratios of 5,000 are measured. The background generated there has its origin in splitting, trapping, or escape of charge produced at the radiation entrance window. It covers the complete surface homogeneously and consists of an Aluminum coating with a thickness of 30 nm and a p$^+$ implant in the Silicon bulk. The effects caused by the entrance window are not treated here, but are subject of previous [8,9,10] and further investigations, using synchrotron radiation in the soft x-ray range and an SDD without Beryllium entrance window.

More detailed spot measurements are performed with a much smaller spot

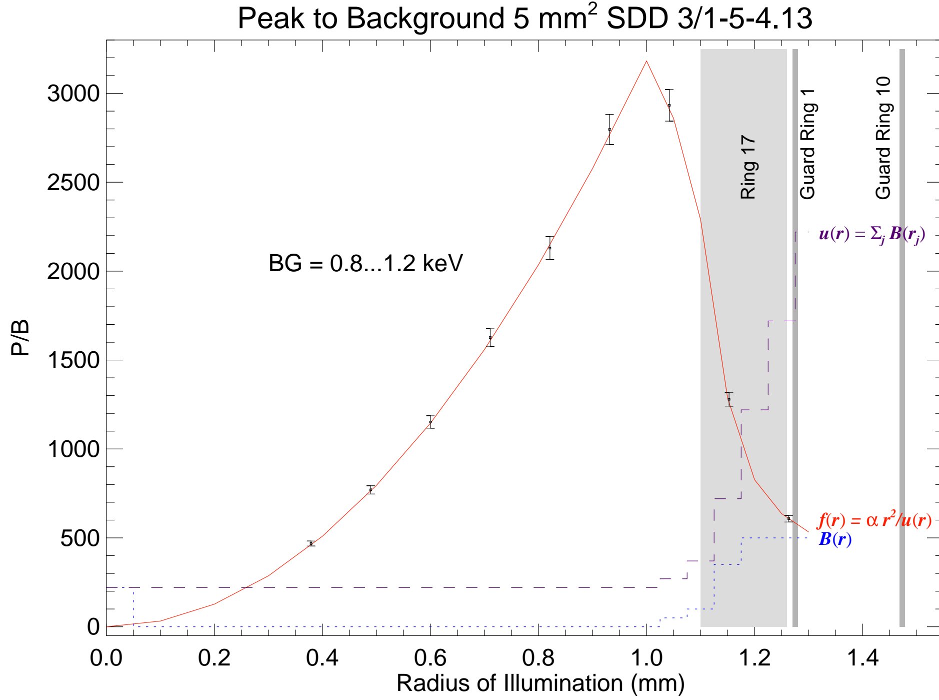

Fig. 2. Peak-to-background p/b vs. r_i (dots with error bars). Solid line: fit function f, dotted line: local background function B, dashed line: total background u (see definitions in section 4.3).

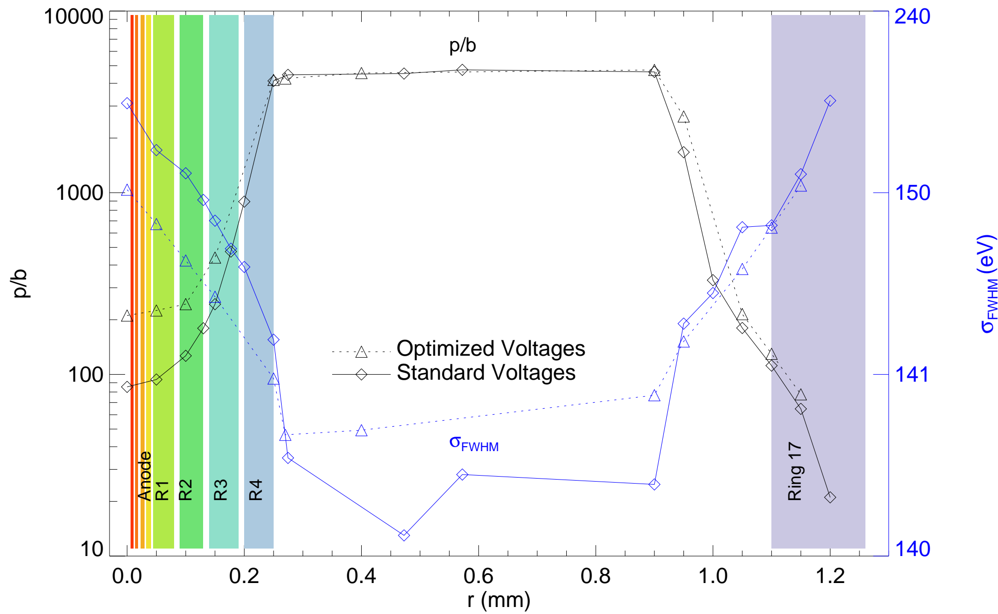

Fig. 3. Peak-to-background ratio p/b (left axis, π-shaped graph) and energy resolution σ_FWHM (right axis, v-shaped graph) in log scales versus the position of the x-ray spot.

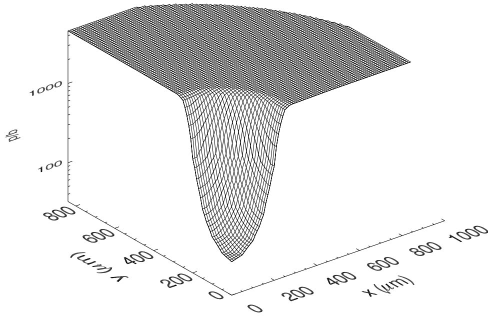

Fig. 4. 3D visualization of the p/b measurements with standard voltages. View from the read-out node ($x = 0$, $y = 0$). The z axis is a log scale.

diameter of about 150 μm (FWTM). The spot positions range from $r = 0$ to $r = 1.2$ mm. Several different detector voltages are applied in order to find the optimum values for good energy resolution, p/b ratio, and ω.

The first measurements are taken with bias voltages optimized for energy resolution, using the standard inner guard ring voltage of -15 V and the standard collimator size ($r_c = 1.2$ mm). The results are indicated by $\diamond$ in fig. 3.

The spot measurements are then repeated for several different bias voltages, which change the electric field within the SDD, in order to investigate the effect of the potential distribution on the probability of partial event generation.

The best values for p/b, ω, and σ_{FWHM} are obtained with the voltage changes given in table 1. The results for the illumination with a small spot size are indicated by $\triangle$ in fig. 3. The actual effects of the voltage changes are treated in section 5.

In fig. 3, the results of measurements with standard and optimized voltages are compared. The peak-to-background ratio p/b (left axis) and the energy resolution σ_{FWHM} (right axis) are shown versus the position r of the x-ray spot. The solid lines indicate the measurements with the standard bias voltages (i.e., optimum resolution without additional collimator), the dotted lines indicate the measurements with voltages optimized for both, resolution and p/b. As the results are displayed logarithmically, the energy resolutions from $r = 0.25$ mm to 0.95 mm obtained with the optimized voltages ($\sigma^{\mathrm{min}}_{\mathrm{FWHM}} = 140.7$) seem to be worse than the energy resolution achieved with the standard voltages ($\sigma^{\mathrm{min}}_{\mathrm{FWHM}} = 140.1$). However, the energy resolutions are practically equal within errors.

Table 1
Net voltages for standard settings and optimized for high p/b: The first (R 1) and last drift ring (R 17), the inner guard ring (IGR), and the back contact. In addition, the energy resolution and p/b ratio for an illuminated area of $5\,\mathrm{mm}^2$ ($r_c = 1.2$ mm), and p/b for an illuminated area of about $3\,\mathrm{mm}^2$ are given (see figures 5 and 6).

	Standard	Optimized
R 1 (V)	−7.3	−5.3
R 17 (V)	−68	−57
IGR (V)	−15	−20
Back (V)	−54.5	−53.0
$\sigma^{\mathrm{FWHM}}_{5\,\mathrm{mm}^2}$ (eV)	144	144
$p/b_{5\,\mathrm{mm}^2}$	550	570
$\sigma^{\mathrm{FWHM}}_{3\,\mathrm{mm}^2}$ (eV)	142	141
$p/b_{3\,\mathrm{mm}^2}$	2,930	3,520

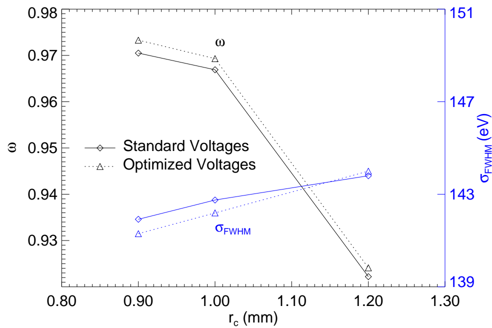

Fig. 5. Left axis, lines with negative slope: ω, right axis, positive slope: σ_{FWHM} for three collimator radii r_{c}. Standard ($\diamond$) and optimized ($\triangle$) voltages (s. table 1).

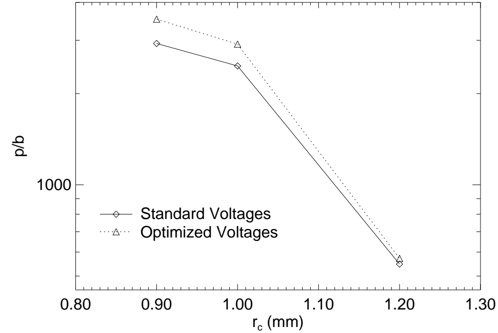

Fig. 6. p/b vs. collimator radii for the same measurements as in fig. 5 on a log scale.

The shaded subjacent rectangles show the positions of the read-out node, the drift rings $1 \ldots 4$, and the last drift ring (ring 17). Note that the spot radius is $75\,\mu$m (FWTM), so the optimum p/b values are already reached at $r_{\mathrm{min}}^{\mathrm{opt}} = (250 - 75)\mu$m $= 175\,\mu$m (beneath the third drift ring) and last till $r_{\mathrm{max}}^{\mathrm{opt}} = (900 + 75)\mu$m $= 975\,\mu$m.

The net biasing voltages applied to the SDD and the resulting energy resolution and p/b ratios are given in table 1. If the active area of the SDD is completely illuminated, the optimized voltages yield only a small improvement of p/b of about $4\,\%$. If the outer region is masked, they lead to an improvement of $20\,\%$. Although this is not an exceptional improvement, it is nevertheless significant, as the enhancement is solely achieved by a change of the voltages and not by a modified layout or technological process.

A rectangular slice of the device is shown in the 3D illustration of the p/b measurements in fig. 4. The area with excellent ω and p/b (about $3\,\mathrm{mm}^2$) is much larger than the inner ($0.1\,\mathrm{mm}^2$) and outer ($1.9\,\mathrm{mm}^2$) areas with low ω and p/b.

The improvements by applying the optimized voltages for small and large collimator radii are shown in fig. 5 (ω and σ_{FWHM}) and and fig. 6 (p/b). For these measurements, not small apertures but additional collimators as in section 4.1 are used to reduce the illuminated area πr_{c}^2, as is the case for usual operating conditions of the SDD.

4.3 The model

A model is developed to describe the behavior of p/b for different radii of illumination, and to identify the regions of partial event generation. As a first estimate, the function $f(r_{\mathrm{i}})$ describing p/b vs. r_{i} scales solely with the illuminated area: As the partial events are assumed to be mainly produced underneath the read-out node in the center of the chip, and its contribution to the total illuminated area becomes smaller with larger r_{i}, the first estimate of f is only propor-

tional to r_i^2 and a scaling factor α.

With this simple assumption, it is not possible to adapt α in a way that $f(r_\mathrm{i})$ reproduces the p/b values both at low r_i ($\leq$ 0.8 mm) and at high r_i. Thus, $\alpha\, r_\mathrm{i}^2$ is divided by a position dependent, discrete total background function $u(r)$, which gives the amount of partial events produced over the complete illuminated area:

$$f(r_\mathrm{i}) = \frac{\alpha\, r_\mathrm{i}^2}{u(r_\mathrm{i})} \tag{2}$$

$$u(r_\mathrm{i}) = \sum_{j=0}^{i} B_j(r_\mathrm{i}) \tag{3}$$

$B(r)$ is an empirical and discrete "local" background function. $B(r_\mathrm{i})$ is altered from its initial value 0 only where it is necessary to fit the data points, i.e., at $r_\mathrm{i} = 0$ and from $r_\mathrm{i} = 1.05$ mm to 1.3 mm. Both $u(r_\mathrm{i})$ and $B(r_\mathrm{i})$ have a stepping of 50 μm.

With $B(r_\mathrm{i})$ becoming larger beneath the last two drift rings, where the electric potential is relatively flat, f reproduces the measured p/b ratios very well. However, the shape of B cannot be easily understood using a simple analytical expression.

This model shows that the data can be explained by three regions of partial event generation:

- The region beneath the readout node (described by B at $r_\mathrm{i} = 0$ mm);
- The region beneath the outmost drift rings (B at $r_\mathrm{i} > 1$ mm).
- The radiation entrance window (described by α)

Although this model gives a first indication, where the partial events are created, a better understanding of the charge splitting is obtained by a calculation of the SDD's distribution of the electric potential.

5 Calculation of the potential distributions

The simulation of the SDD's electric potential is performed in three steps: At first, the technological procedures during the production are simulated to obtain accurate doping profiles, particularly with regard to the transistor region. These profiles are then used to calculate the electric potentials of the complete SDD. Finally, the potential distribution of the inner region of the SDD is simulated with a high resolution.

The doping profiles of the front side (transistor, drift rings, guard rings) are simulated, whereas the doping profiles of back side (back contact) are taken from a SIMS measurement of a similarly processed wafer. The simulation of the doping profiles is realized by considering the mask geometries, as well as all etching, doping, annealing, and deposition processes. It is performed by using the DIOS program [11,12].

In fig. 7, the electric potential distribution of the SDD is plotted. The simulations of the electric potential are performed using the WIAS-TeSCA package [13]. The electrons drift to the most positive potential, that is the anode. The holes are at-

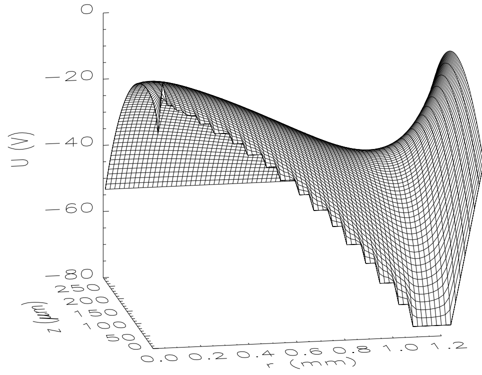

Fig. 7. Distribution of the electric potential within the SDD. The full device is shown. The electrons drift to the most positive potential. The potential decreases from the innermost ($r = 0.05$ mm) to the outermost drift ring ($r = 1.2$ mm). At $r > 1.3$ mm, the potential increases again.

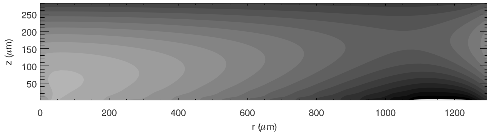

Fig. 8. Contour plot of the electric potential (r and z axes are to scale). Darker regions indicate a more negative potential. The position of the "drift channel" is located at the minima of the parabola-shaped equipotential curves.

tracted by the most negative potential, that is the back side and the drift ring contacts. In fig. 8, the contour plot of the electric potential, the "plateau" region at $r \approx 1.1$ mm, $z \approx 0.2$ mm and the drift channel can be located more precisely than in the 3D-plot.

For the calculation of the potential distribution at the center of the SDD, the device is not simulated with its actual size ($r = 1.3$ mm, $z = 280\,\mu$m), but with all original dimensions except the number of drift rings (6 instead of 17), yield-

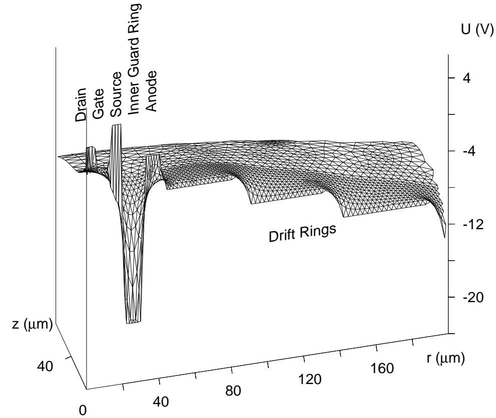

Fig. 9. Potential distribution at the center of the SDD. The depth z is only shown from $0 \ldots 80\,\mu$m. From left to right: JFET (drain, gate, source), inner guard ring, anode, drift rings.

ing $r = 425\,\mu$m, $z = 280\,\mu$m, which results in an active area of about $0.5\,\mathrm{mm}^2$.

The high-resolution potential distribution is shown in fig. 9 (view from the front side). The potential at the anode is about 0 V. The positive voltages applied to the JFET (source, drain) are shielded by a negative potential at the inner guard ring. Thus, the electron clouds drift to the local potential maximum, i.e., mainly to the anode.

By an increase of both, the voltages at the innermost and the outermost drift rings, a higher number of electrons clouds produced underneath the transistor region are completely driven to the anode. An even higher peak probability is obtained, when the shielding of the transistor is enhanced, by applying a more negative potential to the inner guard ring and by an additional adjustment of the back voltage.

6 Conclusions and outlook

Three different regions of partial event generation are located: the radiation entrance window, the transistor area, and the region beneath the outmost drift ring. In all these cases the partial charge loss is produced by splitting the charge cloud at the minimum of an electric potential. The partial charge loss produced at the entrance window is not covered here, but is subject to further investigation.

The partial events produced beneath the the transistor region are caused by a splitting of the charge cloud at the inner guard ring. Similarly, the charge cloud can be split up, when it is produced underneath the outmost drift ring.

By applying a more positive voltage to the drift rings and a more negative voltage to the inner guard ring, it is possible to reduce the number of background events beneath the JFET and the outmost drift ring. However, the charge loss by electrons going directly into the JFET cannot be suppressed totally. This charge loss can only be prevented completely when the read-out structure is not illuminated, as it is the case for asymmetrically shaped SDDs (SDD "droplet", SD^3).

The background events produced beneath the outer ring can easily be reduced by a collimator with a smaller radius, which is either mounted to the housing, or directly glued onto the chip. The advantage of the latter configuration is that the illuminated area does not depend on the geometrical configuration. The feasibility of attaching a collimator with a thickness of 0.5 mm to the chip surface was already successfully tested.

A further improvement of the p/b ratio is realized, when a $10\,\mathrm{mm}^2$ SDD with an illuminated area reduced to about $7\,\mathrm{mm}^2$ is used. Its transistor region occupies the same area as on a $5\,\mathrm{mm}^2$ SDD, but the overall active area is much larger, thus peak-to-background values of up to 6,000 are obtained.

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