High stability X-ray spectroscopy system with on-chip front-end in charge amplifier configuration

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Abstract

The paper presents the performance of a two-chips detector system based on a silicon drift detector and on a charge amplifier, part of the latter being integrated in the detector chip. The two-chips system is intended for high resolution X-ray spectroscopy experiments in which stability of operation is mandatory to avoid on-line calibration procedures. Experimental measurements have been carried out to test the stability of the whole system with a quantitative analysis of the gain stability obtained by comparing X-ray spectra taken at different operating conditions, varying the temperature and/or the detector bias. A gain variation of less than 0.4% has been obtained at extreme operating conditions. The problems and critical aspects of the two-chip charge amplifier solution are discussed.

Keywords: Front-end electronics; Charge amplifier; X-ray detectors; X-ray Spectroscopy; High stability

1. Introduction

In the last decade big efforts have been devoted to enhance the energy resolution of silicon detectors while extending their active area. This trend has lead to the development of silicon drift detectors and their parental devices [1-3] and to the integration of the first stage of the front-end electronics in the detector chip [4, 5].

Our work follows this trend and aims to improve, with respect to the available solutions, the stability of the charge-to-voltage conversion when temperature and/or bias may vary during the experiment. This feature avoids the periodic re-calibration of the system and may be interesting in long-lasting measurements and in multi-channel systems, where continuous re-adjustment is difficult or impractical. To accomplish this task, we have chosen a charge amplifier configuration in order to profit by the stability of the feedback capacitance in the charge-to-voltage conversion.

The first stage of the front-end has been partially integrated in the detector chip to minimize the parasitic capacitances at the anode and to avoid microphonisms [6]. A "Boltzmann emission"-based reset mechanism, performed by a BJT or a MOSFET

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operating in weak inversion regime, has been designed to reach better linearity of discharge and lower noise with respect to a strong inversion MOSFET [7].

The schematic of the charge amplifier is shown in Fig. 1. All the devices directly connected to the anode, i.e. the front-end nJFET, the feedback capacitance and the reset device are integrated on the detector chip. The transimpedance amplifier that completes the charge amplifier, is bonded to the detector chip.

2. The detector chip

The design of the detector chip [6] has to face the technological constraints associated with the limited technological steps optimized for the detector production. The detector starting material is a high-resisitivity (2 kΩ · cm) n-type silicon wafer 280 μm thick. The front-end nJFET is located inside a p^+ guard ring in reverse bias with respect to the detector

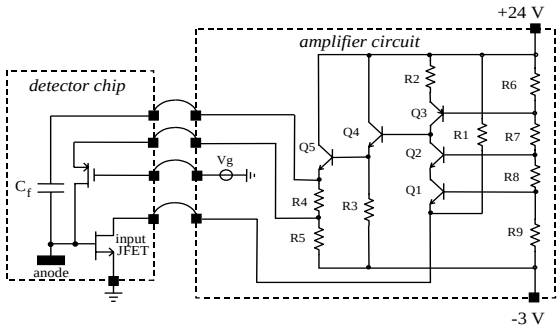

Fig. 1 Schematic of the charge amplifier. The amplifier circuit contains a transimpedence circuit that drives the feedback capcitance and the reset device integrated on the detector chip.

anode ring. The reset device is embedded within the front-end JFET and the feedback capacitance (50 fF) is obtained with a metal contact over the nitride layer placed on top of the anode ring implant. See [6] for more details. The design of the feedback capacitance has been optimized to reduce the contribution of stray capacitances to less than 1% in order to guarantee a high degree of stability of the charge-to-voltage conversion factor. The presence of the devices embedded within the anode ring does not affect its symmetry and, therefore, the collection of the electrons.

The DC characteristics of both the input nJFET and the reset transistor have been measured with both the devices properly biased, so as the detector, in order to test the joint operation of the detector embedded front-end. The JFET saturation current is 980 μA, the transconductance at 4.5 V drain-to-source voltage and 0 V gate-to-source voltage is about 380 μA/V and the dynamic output resistance is 15 kΩ.

3. The reset mechanism

3.1. Principle of operation

The electrons collected at the anode are compensated by means of a “Boltzmann emission”-based reset transistor in the feedback loop whose cross section, in the pMOSFET implementation, is shown in Fig. 2. The transistor is DC coupled and therefore performs a continuous reset, injecting holes into the JFET gate, which is directly connected to the detector anode. Two “Boltzmann emission”-based reset transistors have been designed: a pnp BJT and a pMOSFET operated in weak inversion regime. The reset transistor is embedded in the JFET structure and has the Source (Emitter in the BJT version) connected to the output of the preamplifier circuit and the Drain/Collector being the p+ implant of the nJFET gate. In the case of the MOSFET, the Gate is held at a fixed voltage that guarantees weak inversion operation. In the case of the BJT, the base is constituted by the nJFET channel implant and cannot be directly accessed. The MOSFET solution can prevent the introduction of parasitic transistors as it does not require the forward bias of the Source/Emitter contact.

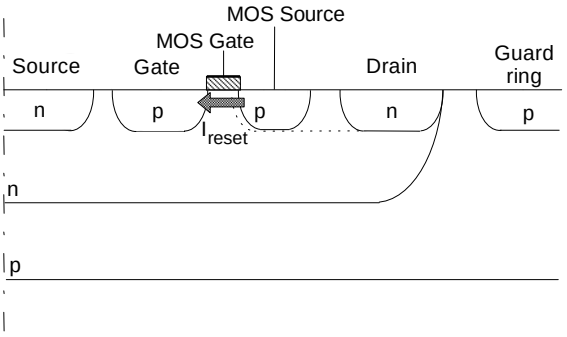

Fig. 2 Cross section of the inner part of the detector chip, taken radially through the reset device in the MOSFET version. The reset mechanism is obtained by the injection of holes from the MOSFET source into the JFET gate, directly connected to the detector anode.

3.2. DC operation of the reset pMOSFET

The transfer characteristic curves of the reset pMOSFET are shown in Fig. 3. The curves have been measured when both the JFET and the pMOSFET were properly biased with the MOSFET drain at –1.5 V. The weak inversion regime (exponential dependence between I_D and V_S) and the strong inversion regime (quadratic dependence) can be clearly distinguished. In the weak inversion regime we have

$$I_D \propto exp\,[V_{SG} / (nV_{TH})] \quad (1)$$

where V_{TH} is the thermal voltage, equal to 25 mV at

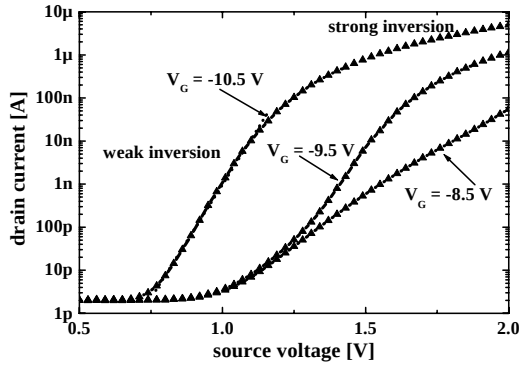

Fig. 3 Transfer characteristic curves of the reset MOSFET, obtained holding the MOSFET Drain at –1.5 V.

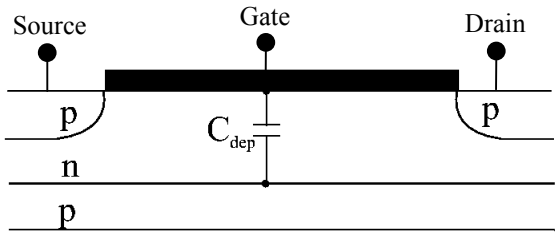

Fig. 4 Schematic view of a pMOSFET operating in weak inversion regime, showing the capacitive division responsible for the *n* factor.

room temperature. The *n* factor accounts for the capacitive division between the gate oxide and the depleted bulk as shown in Fig. 4 and is given [7] by

$$n = 1 + C_{DEP} / C_{OX} \quad (2)$$

The threshold gate-to-source voltage between the two regions is about –12 V, while *n* is equal to 1.6.

3.3. Self-adaptation to leakage current variations

The non-linear dependence between current and voltage of the reset device actually makes the dynamic resistance depending on the leakage current I_L. Therefore, the discharge time constant τ reduces as the total amount of leakage current circulating in the reset device increases, according to

$$\tau = C_F / g_m = C_F\, nV_{TH} / I_L \quad (3)$$

The dynamic range for leakage current compensation is intrinsically high thanks to the logarithmic relation between the source voltage and the drain current. Fig. 5 shows the relation between the Source (or Emitter) voltage and the discharge time constant, related to the total amount of leakage current according to Eq. (3). The measurement (dots in the figure) has been carried out by varying the amount of visible light impinging on the detector and therefore the leakage current. Variations of up to 4 orders of magnitude in the total amount of leakage current are accommodated with a change of less than 200 mV in the output bias voltage. The difference between the slopes of the fitting for the MOSFET and the BJT reset is due to the value of the *n* factor. The functional similarity of the two curves certifies that

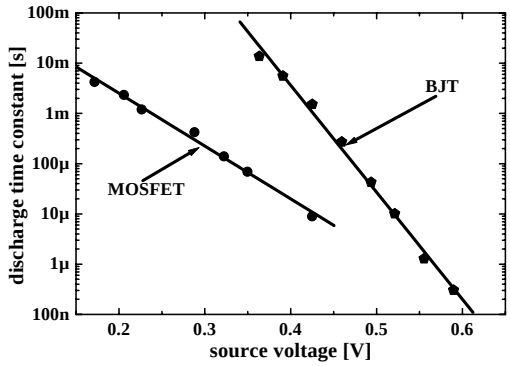

Fig. 5 Discharge time constant (related to leakage current) versus the DC output voltage when a MOSFET or a BJT is used as reset device. The relation is exponential for both systems, certifying that the MOSFET is operating in weak inversion regime. The difference in slope is due to the capacitive division between the gate oxide and the depleted bulk existing only in the MOSFET.

the MOSFET is actually operating in the weak inversion regime.

4. The amplifier circuit

The schematic of the transimpedance amplifier circuit is shown in the right part of Fig. 1. The transistors Q1 and Q2 are connected in common-base configuration to form a double cascode in order to minimize the input dynamic resistance of the transimpedance amplifier. The resistor R1 supplies most of the bias current of the front-end nJFET, but its dynamic effect is negligible as it is in parallel with the resistance $1/g_{m1}$ at the emitter of the double cascode. Q3 and R2 form the active load of the stage, designed to maximize the transimpedance θ of the amplifier circuit that makes the current-to-voltage conversion of the JFET drain current. The amplifier is completed by the follower stages Q4 + R3 and Q5 + R4 + R5. The ratio R4 / R5 has been chosen in order to insure the correct bias of the reset device.

The midband loop gain of the charge amplifier is equal to

$$G_{loop} = - g_m \cdot \theta \cdot C_F / C_{TOT} \quad (4)$$

where C_{TOT} is the sum of all the capacitances connected to the detector anode (feedback C_F, detector, JFET gate and parasitics), and g_m is the transconductance of the input JFET.

According to the feedback circuit theory, the stability of the overall charge-to-voltage conversion factor *G* is given by

$$dG / G = (dG_{fw} / G_{fw}) / (1 - G_{loop}) \quad (5)$$

where $G_{fw} = g_m \cdot \theta$.

In order to achieve the maximum stability of the charge-to-voltage conversion the following two requirements must be fulfilled: 1) the amplifier circuit must guarantee an adequate value of the loop gain, despite the low transconductance of the input nJFET and therefore θ has to be high; In our case the loop gain is higher than 200. 2) the term G_{fw} should be highly stable. With a hybrid amplifier circuit and no constraints on the value of the power supply it can be easy to have a percentual variation of θ much lower than the JFET transconductance variation whose temperature variation is of the order of 1%/K.

In a VLSI amplifier integrated in standard technology problems may arise due to the limited value of the maximum certified bias voltage (typically of 5 V) that prevents the use of a double-cascode and forces R2 to be low.

Another keypoint for the amplifier circuit is the noise constraint. The added noise of the transimpedance amplifier must be negligible with respect to the input JFET noise. The main noise contribution of the transimpedance amplifier arises from the low output resistance of the input nJFET, which can introduce part of the noise of the input transistor Q1 and of the resistors used for the voltage references.

5. System performance

5.1. Stability of Amplification

In order to test the stability of the charge-to-voltage conversion versus detector bias and temperature, ^{55}Fe spectra have been acquired at different bias voltages and operating temperature and the corresponding peak shifts (the Mn Kα peak has been considered) have been measured.

Fig. 6 shows the measured values of the peak shift versus the bias voltage of the p^+ guard ring that surrounds the nJFET and insulates it from the detector anode. Despite the fact that any variation of its bias would change significantly the detector capacitance (i.e. the capacitance reduces as the bias voltage increases), a variation of about 60% of the bias voltage leads to a peak shift of only 0.15%.

In the second set of measurements, the operation temperature has been varied in the ranges 0 - 20 °C and 30 – 40 °C. Any variation in the operation temperature changes a number of parameters, such as the detector and JFET capacitances, the current flowing in the front-end JFET, its transconductance and the transimpedance gain. Nethertheless Fig. 7 shows that the peak shift measured at different temperatures is only of the order of 0.2% every 10 °C.

The high degree of stability that may be reached in a given charge amplifier configuration, provided that the feedback capacitance value is stable, is given by Eq. (5) which demonstrates that only a fraction of the variation of the detector parameters reflects on the total charge-to-voltage conversion factor. In our case, the measured residual peak shift is mainly due to the variations of the forward gain, G_{fw}, directly related to the devices on the detector chip, not compensated by a sufficiently large loop gain of the external amplifier.

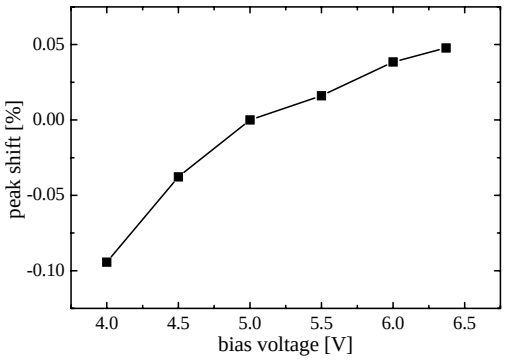

Fig. 6 Relative peak shift varying the p^+ guard ring bias voltage. A variation of less than 0.15% in the peak position has been measured with respect to a variation of 2.5 V in the bias voltage.

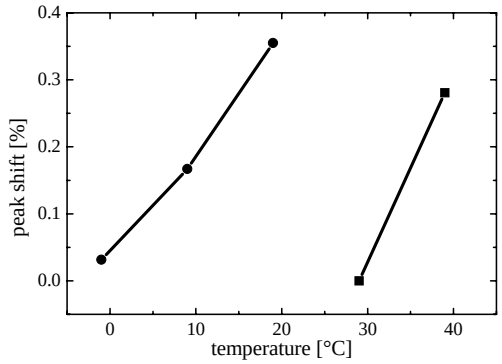

Fig. 7 Relative peak shift varying the operation temperature. A variation of 10 °C in the temperature causes a peak shift of about 0.2%. The two curves do not connect because the bias has been varied between the two experiments.

5.2. Energy resolution

The resolution of the system has been measured at room temperature (300 K). Fig. 8 shows the energy spectrum of a ^{55}Fe source acquired at the optimal shaping time (1 μs). The measured energy resolution is 252 eV FWHM at the Mn Kα line, corresponding to an ENC of 26 electrons rms.

The obtainable resolution is limited by the excess noise of the front-end nJFET, that shows a value of A_f of $1.1 \cdot 10^{-11}$ V^2 (see Fig. 9). Such value of A_f is about an order of magnitude higher than the measured values for similar JFETs in previous productions [9].

In order to confirm that the resolution value is due to the excess noise of the front-end nJFET and not to the charge amplifier set-up, the same “detector chip” has been connected in source follower configuration. Indeed, the ENC has been measured to be 25 electrons rms when the feedback capacitance is left floating (thus minimizing the total anode capacitance) and 25.9 electrons rms when it is connected to ground (thus showing the same anode capacitance of the charge amplifier configuration).

6. Conclusions

The experiments taken on the proposed X-ray spectroscopy system performing a charge amplification confirm the validity of the project.

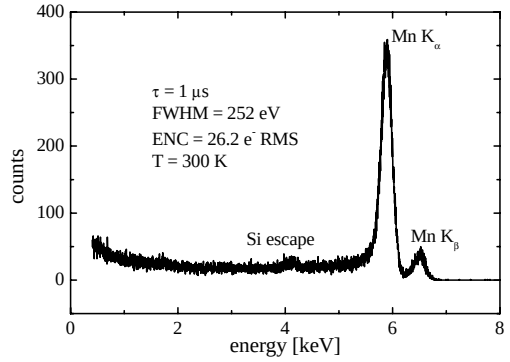

Fig. 8 Energy spectrum of a ^{55}Fe spectrum acquired at room temperature at the optimal shaping time (1 μs). The measured resolution is 252 eV FWHM, corresponding to an ENC of 26.2 electrons rms. The silicon escape peak at 4.15 keV is also visible.

Stabilities below 0.4% have been reached at extreme operating conditions, obtaining the same energy resolution with respect to the source follower configuration.

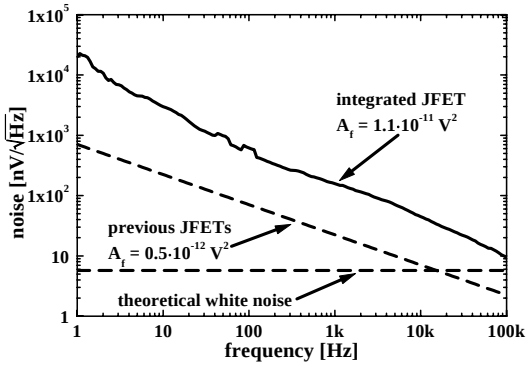

Fig. 9 Noise spectrum of the front-end nJFET. The high value of A_F is the main responsible for the ENC introduced by the electronics.

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References

[1] P. Lechner, S. Eckbauer, R. Hartmann, S. Krisch, D. Hauff, R. Richter, H. Soltau, L. Strüder, C. Fiorini, E. Gatti, A. Longoni, M. Sampietro, Nucl. Instr. and Meth. A 377 (1996) 346

[2] H. Soltau, P. Holl, J. Kemmer, S. Krisch, C. v. Zanthier, D. Hauff, R. Richter, H. Bräuninger, R. Hartmann, G. Hartner, N. Krause, N. Meidinger, E. Pfeffermann, C. Reppin, G. Schwaab, L. Strüder, J. Trümper, E. Kenziorra, J. Krämer, Nucl. Instr. and Meth. A 377 (1996) 340

[3] A. Castoldi, E. Gatti, C. Guazzoni, A. Longoni, P. Rehak, L. Strüder, Nucl. Instr. and Meth. A 439 (2000) 519

[4] V. Radeka, P. Rehak, S. Rescia, E. Gatti, A. Longoni, M. Sampietro, G. Bertuccio, P. Holl, L. Strüder, J. Kemmer, IEEE Electron Device Lett. 10 (2) (1989) 91

[5] J. Sonsky, R.N. Koornneef, L.K. Nanver, G.W. Lubking, J. Huizenga, R.W. Hollander, C.W.E. van Eijk, Nuclear Science Symposium Conference Record, 2000 IEEE, (2000) 9/204 - 9/208.

[6] C. Guazzoni, M. Sampietro, A. Fazzi, P. Lechner, IEEE Trans. Nucl. Sci. 47 (4) (2000) 1442

[7] C. Guazzoni, M. Sampietro, A. Fazzi, Nucl. Instr. and Meth. A 443 (2000) 447

[8] D. A. Johns, K. Martin, Analog Integrated Circuit Design, John Wiley & Sons, 1997, p. 41

[9] M. Sampietro, L. Fasoli, G. Bertuccio, IEEE Trans. Nucl. Sci. 43 (4) (1996) 2413

[10] P. Rehak, S. Rescia, V. Radeka, E. Gatti, A. Longoni, M. Sampietro, G. Bertuccio, P. Holl, L. Strüder, J. Kemmer, U. Prechtel, T. Ziemann, Nucl. Instr. and Meth. A 288 (1990) 168