

Active Pixel Sensors for Imaging X-ray Spectrometers

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ABSTRACT

Active Pixel Sensors (APS) offer high-resolution imaging in combination with a fast and flexible readout. The MPI Halbleiterlabor develops and produces DEPFET (**D**epleted **F**ield **E**ffect **T**ransistor, [1]) based APS devices. They are additionally characterized by enhanced sensitivity for X-ray photons in the range from 0.1 keV to 25 keV, spectroscopic energy resolution (below 1 electron r.m.s.) and radiation hardness. Moreover, the production process on high-ohmic silicon allows incorporating additional high-speed spectrometers based on silicon drift detectors. Such a detector system is proposed as a wide field imager for the XEUS (X-ray Evolving Universe Spectroscopy) mission. XEUS is a planned project within the European Space Agency's Horizon 2000+ program. We will present a focal plane concept for XEUS and measurement results from DEPFET-APS prototypes and high speed drift detectors.

Keywords: pixel detectors, CCDs, XEUS, XMM-Newton, drift detectors, X-ray, imaging, spectroscopy

1. INTRODUCTION

Today's most advanced X-ray space telescopes – Chandra and XMM-Newton – use several different CCD based systems for X-ray spectroscopy and imaging. Among those the XMM pn-CCD camera [2] combines the best quantum efficiency with the fastest readout and highest radiation hardness. Still, the maximum photon rate with this instrument is limited by pile-up to about 10 counts per HEW (Half Energy Width) and second. This number depends on the pixel geometry and is valid for the full frame observation mode and its related timing. The limiting factor is the transfer time of the signals to the readout node, which – in the case of the XMM pn-CCDs – is equal to the readout time. To keep out-of-time events at a tolerable level, integration time is usually chosen at least a factor of 10 longer than transfer time.

The anticipated effective collection area of XEUS will be 6 m² in phase A and 30 m² in phase B, which corresponds to an increase of 40 respectively 200 as compared to XMM's 0.15 m². Moreover the focal length will be increased to 50 m and the HEW improved to 2 arcsec (7.5 m and 13 arcsec for XMM)¹. To cope with the resulting photon rates requires a new detector concept for a wide field imager (WFI). The pn-CCD on XMM could be boosted by adding a frame store region [3] decoupling the readout time from the transfer time. Although this increases transfer speed by a factor of 100 (from 5 ms to 50 μ s for full-frame readout), it does not overcome transfer losses and adds additional active area to the device (e.g. 66 % for the expected XEUS pixel geometry). An APS matrix consisting of DEPFET elements completely avoids any charge transfer and potentially gains another order of magnitude in speed, since only the readout time per pixel (typically 2 μ s) has to be related to the integration time. Out-of-time events, which may still contribute a small fraction of signals, are not geometrically confused.

The random access readout scheme of an APS also adds more flexibility allowing a large variety of observation modes dedicated to particular scientific goals. This includes the fast window readout, delivering highly time resolved ($\sim 25 \mu$ s), imaging spectroscopy [4] and a repetitive multi-correlated sampling for enhanced noise-performance. A DEPFET APS also matches the other relevant requirements: position, energy and time resolution as well as quantum efficiency. Its

¹ All optical parameters are specified for 1 keV photons

radiation hardness allows an operation during the expected mission duration without any performance degradation. A functional description is given in section 2; measurement results from prototype devices follow in 3.

A DEPFET APS matrix has therefore been suggested as a WFI for XEUS [5] by the MPI Halbleiterlabor, where the detector chip is being developed and fabricated. To match the requirements on XEUS the development focuses on a design with $75 \times 75 \mu\text{m}^2$ pixels and an overall active area of $76.8 \times 76.8 \text{ mm}^2$ corresponding to 1024×1024 pixels and a FOV coverage of more than 5 arcmin. For more details see section 4.

The fabrication bases on the technology developed for the XMM pn-CCDs. It consists of several hundreds steps, including photolithography, ion-implantation, etching, cleaning and thermal treatments. It has been enhanced in many important details: wafer size increased from 4" to 6"; polysilicon, additional metallization and passivation layers have been introduced. Also the 1999 move of the MPI Halbleiterlabor to a new clean room facility has significantly contributed to an improved device performance.

The DEPFET APS is silicon based and converts incident X-ray photons into signal charges by ionization via photo effect (Compton scattering is negligible in the energy range covered by XEUS). This implies an intrinsic limit for the energy resolution due to statistical fluctuation in the charge creation – the so called Fano noise. Far better (up to a factor of 50) spectral resolution is reached with the cryogenic narrow field imagers (NFIs) on XEUS. The NFIs, however, have a restricted field of view in the order of 0.5 arcmin. Hence, the WFI on XEUS will also be an indispensable pathfinder for the NFI.

2. DETECTOR DETAILS

2.1. DEPFET functional principle

The DEPFET pixel consists of a p-channel field effect transistor realized on high-ohmic, n-type silicon. A schematic view is shown in Figure 1/Left. High quantum efficiency results from the uniform and ultra-thin entrance window [7] as well as from the fully sensitive bulk. This is a benefit from the double-sided processing of the wafer allowing a full depletion of the bulk and back illumination. Moreover, an increase of the sensitive thickness from 280 μm (XMM pn-CCDs) to 500 μm further enhances high energy response (see Figure 5 in [8], and [9]).

The *back contact* is a shallow boron implant forming a pn junction. By applying a negative voltage in the order of 200 V all mobile charges are removed from the bulk and an electric field is created. Signal charges, i.e. electron hole pairs, are separated in that field; holes drift to the p back contact where they are drained off, while electrons are collected in a potential minimum below the top surface. That potential minimum – created by high energetic ion implantation – forms the internal gate of the transistor and represents the storage area of the pixel. The transistor current is modulated by the charges in the internal gate and the voltage applied to the external *FET gate*. For a given external voltage at the *FET gate*, the current modulation is a precise measure for the amount of charges stored in the internal gate, i.e. in the pixel. A high precision measurement of the charge is possible due to the extremely small capacitance of the internal gate (~ 50 fF) and the resulting conversion factor of at least 200 pA per electron. Since the stored charges are not affected by the transistor current the readout is non-destructive, which turns the DEPFET structure into a memory cell suitable for random access. However, to reset the device the charges must actively be removed. This is done via the *n+ clear* contact in conjunction with the *clear gate* by applying appropriate voltage pulses.

Single DEPFET pixels can be arranged in a matrix, the principle is shown in Figure 1/Right by a 3×3 pixel subset. In this case a source follower readout is assumed and the sources are connected column-wise, while all drains are connected to a common voltage. The external gates as well as the reset contacts are interconnect row-wise. Using an individual electronic channel to preamplify each column and controlling the row which is active, an unambiguous reading of each pixel is realized. The row-wise activation is achieved by applying a turn-on voltage to all external *FET gates* in one row, while all other rows in the matrix remain turned-off (i.e. their transistor channels are pinched off and no current can flow).

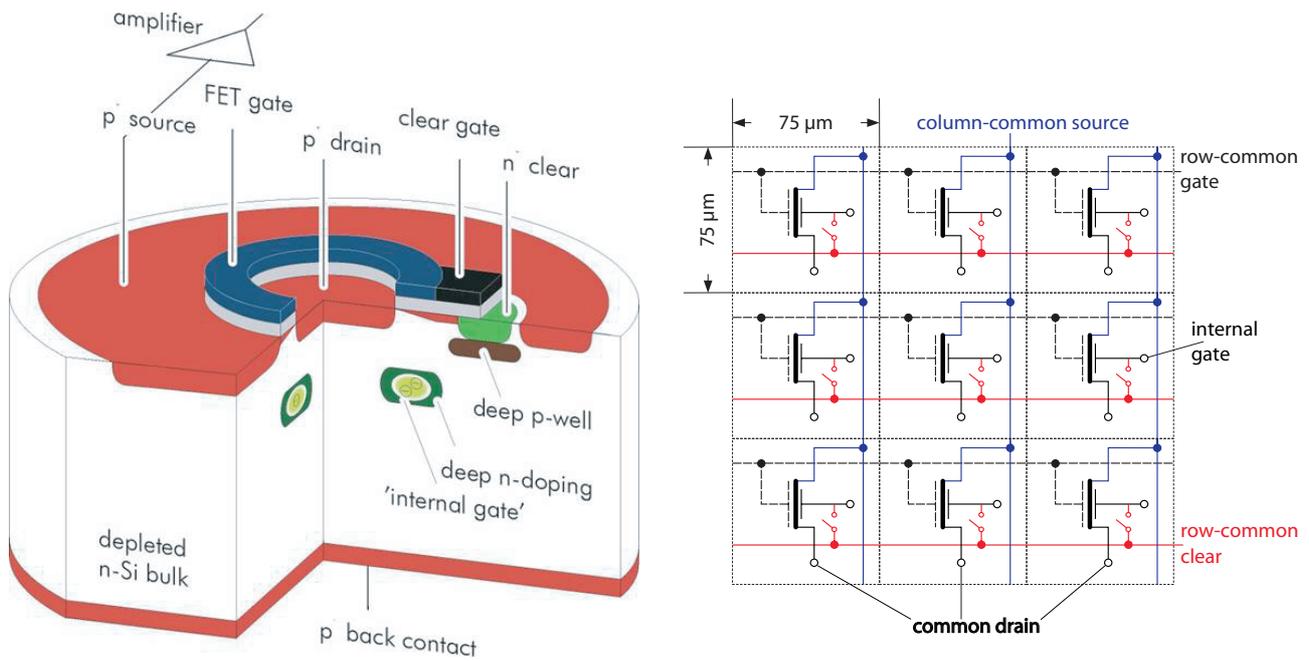


Figure 1, Left: Schematic view of a circular DEPFET pixel. X-ray photons enter through the p back contact. Signal charges are stored close to the opposite (top) side. Right: A 3 × 3 pixel circuitry visualizes how DEPFET pixels are interconnected in an APS matrix.

2.2. Simulation of the DEPFET operating states

For design optimization a large number of device simulations have been calculated with the three dimensional Poisson equation solver POSEIDON, developed by A. Castoldi, E. Gatti and P. Rehak within the INFN-RIMAX project [10, 11]. Figure 2 shows a DEPFET structure in signal integration state. The simulated structure has a circular geometry similar to the one in Figure 1, but the central p+ contact is used as the transistor source and the surrounding p+ ring as the drain. Since a three dimensional potential cannot be pictured in print, we show pairs of two dimensional sections. Their relative locations are indicated: in the right graph a dashed line shows a projection of the left graph's plane and vice versa.

The left plot of Figure 2 shows the potential in a depth of 1 μm parallel to the surface (x-y-plane). The center of the pixel, i.e. the center of the circular external FET gate, is located at x = y = 0. The ring shaped potential maximum (minimum for electrons) corresponds to the internal gate, where the signal charges are stored. In the right plot a cut along x = 0 visualizes the internal gate (at y = ±10 μm) and the n clear contact (between y = 12 μm and y = 28 μm). This section is orthogonal to the surface (y-z-plane). From the right plot also the z-location of the electron potential minimum can be derived: it is at z = 1 μm, where the left plot's section has been placed.

A simulation of the DEPFET structure during reset is shown in Figure 3. A positive voltage applied to the n clear contact removes the potential barrier between the internal gate and the n clear contact. Electrons which were stored in the pixel during integration and readout phase will be completely removed from the internal gate. The removal of all electrons is essential for the performance of the device, since electrons remaining after reset would contribute with the square root of their number to the noise.

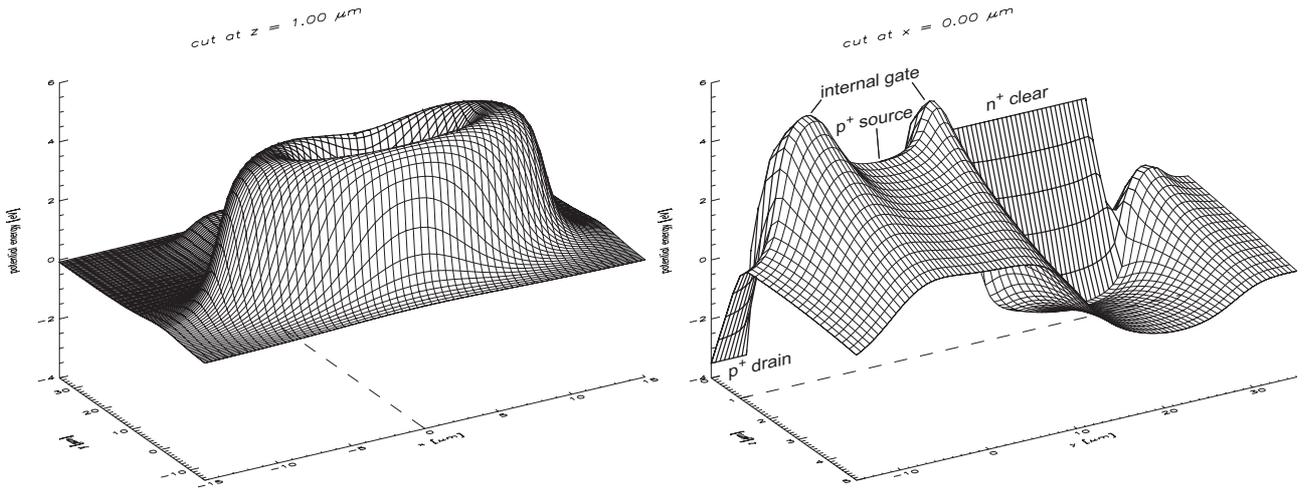


Figure 2: Simulation of the potential in a DEPFET pixel structure during signal integration calculated in three dimensions by the Poisson equation solver POSEIDON. Left: potential parallel to the detector surface in a depth of $1\ \mu\text{m}$. Right: potential perpendicular to the surface.

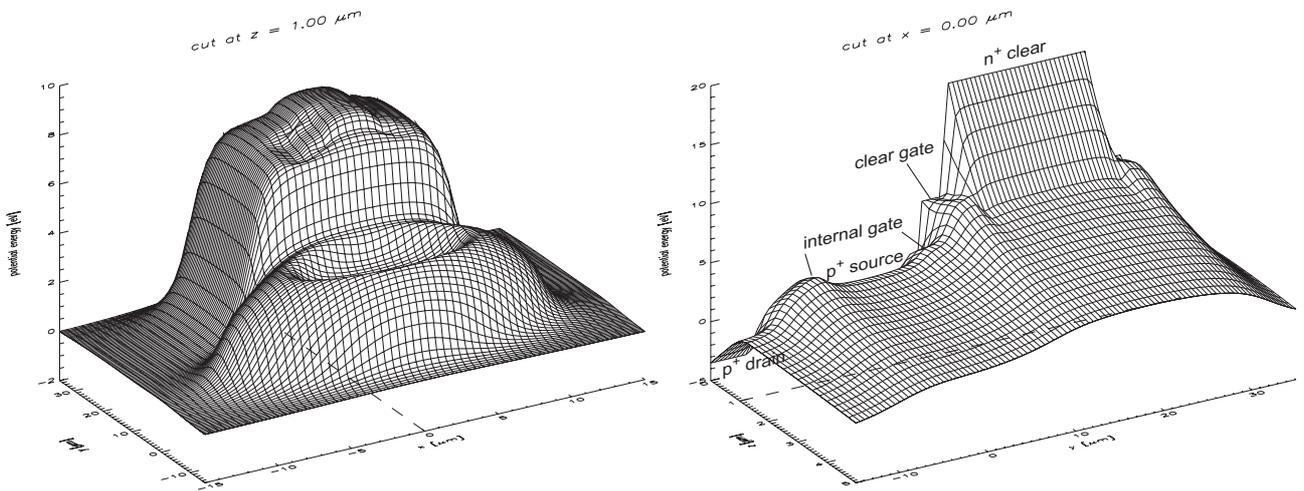


Figure 3: POSEIDON simulation of a DEPFET pixel structure during reset. Again, the left and right plots are different sections through a potential calculated in three dimensions.

2.3. APS system design

As already shown in Figure 1/Right the pixel outputs (sources) are connected column-wise. Each column of outputs is further processed by one channel of a multiplexing preamplifier chip. Figure 4 outlines a complete system including an APS device, control and readout electronics. Every row of pixels is interconnected via their *external gate* and *n clear* contacts. Readout of the matrix is realized row by row, i.e. by turning on the transistor currents via the common *external gate* connection.

For redundancy and performance reasons the 1024×1024 pixel matrix is subdivided in 16 units of 128×512 pixels, each read out by a 128-channel, multiplexing preamplifier chip (CAMEX). Row-wise selection for readout and reset is realized by switcher chips on the left and right sides of the APS. Since the upper and lower 8 subunits are independent two rows (2×1024 pixels) can be processed simultaneously.

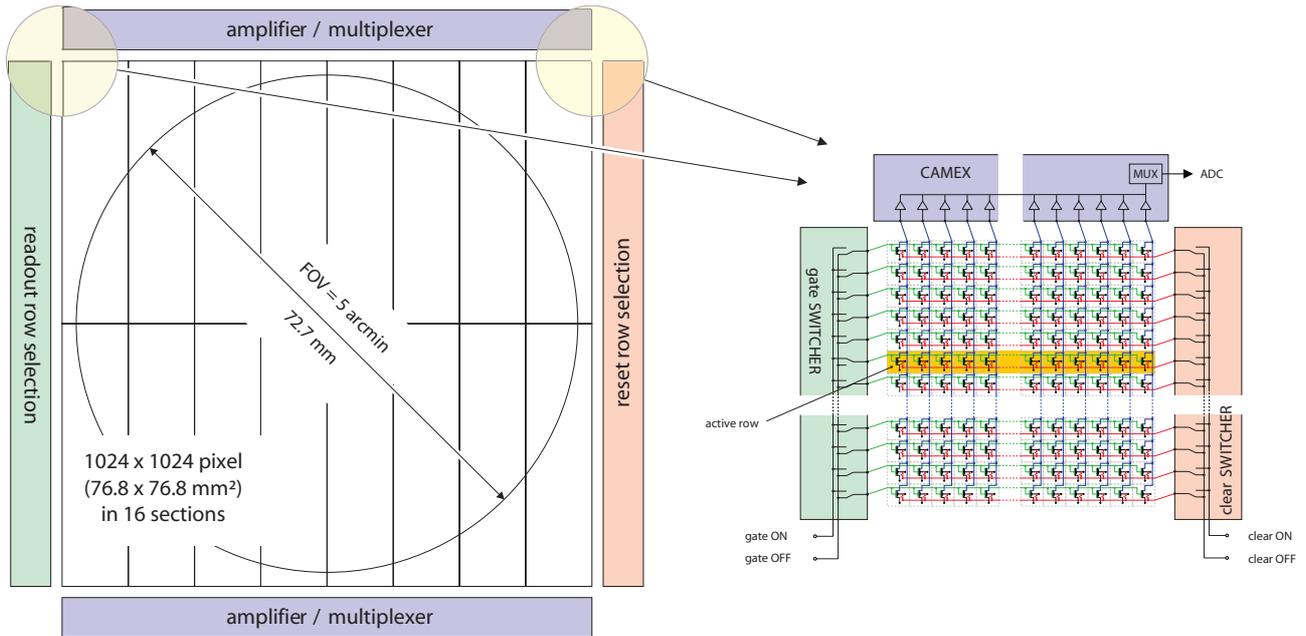


Figure 4: The APS system concept includes readout and steering electronics. The *gate SWITCHER* chips selectively activate single rows of 1024 DEPFEET pixels for readout. The selection of a row to be reset is done by the *clear SWITCHERS*. 16 multiplexing preamplifier chips (CAMEX) receive the signals from the column-wise connected DEPFEET sources.

2.3.1. CAMEX analog amplifier/multiplexer

A new version of the XMM-proven CAMEX chip [12] is being adapted to the requirements of the pixel sensor readout. Now 128 input channels (64 on XMM) are multiplexed into one output. The input stage still uses multi-correlated sampling for noise filtering. The technical innovations include the modification of the CAMEX integrated current source to match the DEPFEET amplifier, the integration of a shift register for the storage of the timing sequence, an enhanced output buffer which is able to run at a frequency of 16 MHz, and a new approach towards the problem of common-mode fluctuations, which is based on the reading of ‘empty’ (i.e. non-connected) channels. Also different filtering techniques are studied and the layout has been modified to fit to the 75 μm pitch of the APS output contacts.

2.3.2. Readout and reset select SWITCHER

For the row by row access the APS system is equipped with the so-called SWITCHER chips. The current version can address 64 rows and has two voltage outputs per row. Two outputs are needed to supply individual pulse levels for the *clear gate* and *n clear* during reset. The timing of the voltage output is controlled by a 256 x 4 Bit RAM sequencer. This allows selecting from four input voltages and switching them to the two currently active outputs. It is fabricated in a high-voltage CMOS technology (AMS0.8 μm “HV”, see [13]) allowing a range from +2 V to +20 V for the *n clear* and *clear gate* and from -15 V to -5 V for the *external gate*.

2.4. Repetitive non-destructive readout (RNDR)

By making use of the non-destructive character of the readout it is possible to further decrease the readout noise contribution. In Figure 5 the principle is shown: two adjacent DEPFEET devices are able to transfer the signal charges from one floating gate amplifier to the neighboring one, reading the same signal charges several times. The read noise is reduced by the square root of n , where n is the number of readings.

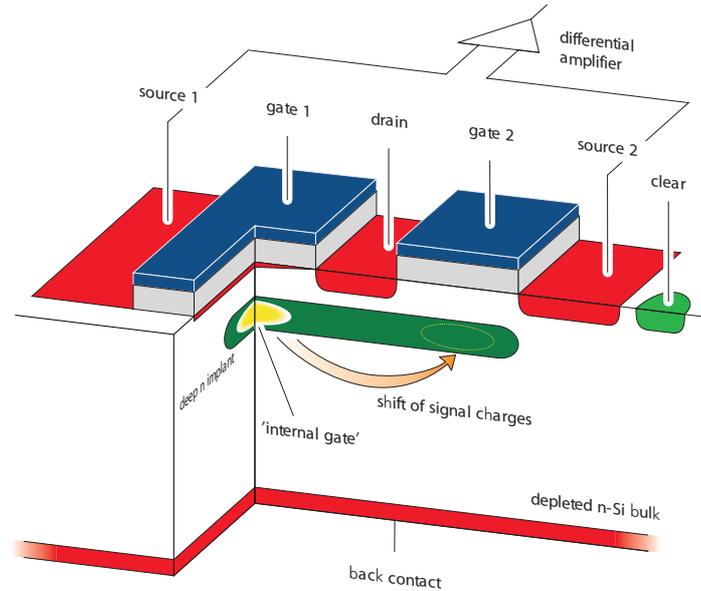


Figure 5: Principle of the repetitive non-destructive readout (RDNR). The pixel is read out n times with the signal charge alternately located in the *internal gate* under *gate 1* and *gate 2*. The theoretically achievable noise reduction is the square root of n .

As the areas which make use of the non-destructive readout can be selected during operation, we imagine to run the detector slowly in areas where faint sources have been detected and fast (without RDNR) where it is not required or not applicable due to high photon rates. Since the Fano noise cannot be reduced by the RDNR method it will mainly improve resolution at the low energy end of the spectrum.

3. PERFORMANCE

3.1. Measurement results

Measurements with a prototype single-pixel structure are shown in Figure 6. It was exposed to a radioactive ^{55}Fe source emitting X-ray photons at 5,894 eV (Mn-K_{α}) and 6,489 eV (Mn-K_{β}). The left spectrum was recorded at ambient temperature and an equivalent noise charge of 8 e^{-} r.m.s. was determined from the dominant Mn-K_{α} peak corresponding to 140 eV FWHM. Cooling to -50°C improves the decreases the noise down to 4.5 e^{-} r.m.s. (130 eV FWHM). The spectra show a relatively high underground which is caused by so-called partial events. They are due to the small area of the single-pixel ($50 \times 50 \mu\text{m}^2$) and occur when the signal charges are not completely collected in the potential minimum. Both measurements were recorded using a continuous time-filter with a shaping time of 6 μs . Measurements on pixel matrix prototypes have been carried out at the University in Bonn [14, 15].

3.2. Expected performance and properties

The described design of the APS pixel matrix and its expected performance is summarized in Table 1.

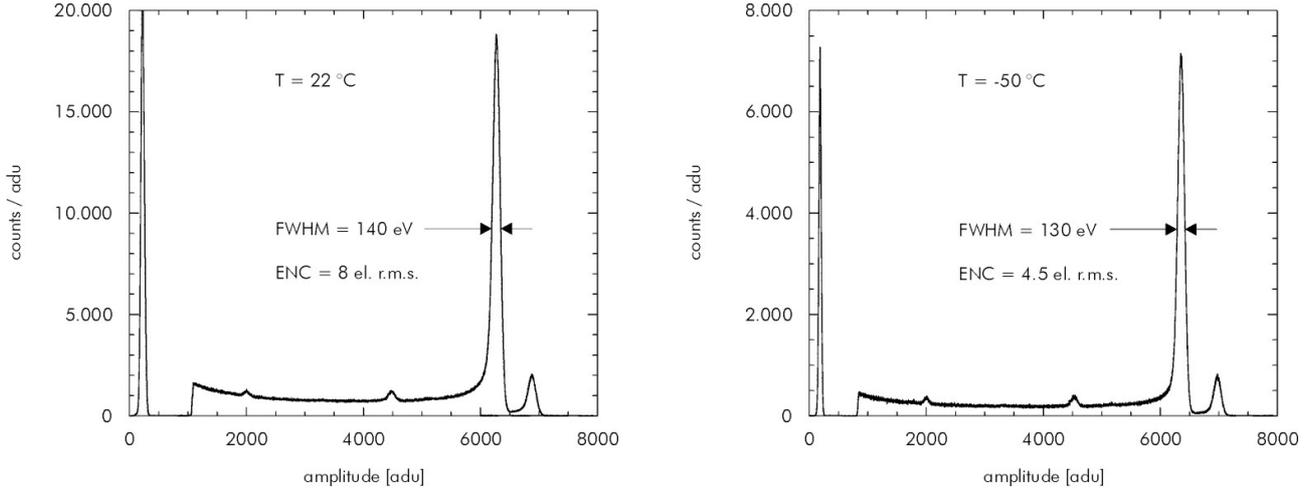


Figure 6: Spectra from a radioactive ^{55}Fe isotope. Left: at ambient temperature; Right: cooled in a climatic chamber to -50°C . FWHM and ENC are indicated for the manganese K_α line.

Pixel size	$75 \times 75 \mu\text{m}^2$
Matrix size	1024×1024 pixels
Logical subdivision	16 (with 128×512 pixels)
Full frame rate	2 ms
Line readout time	$2.5 \mu\text{s}$
Time resolution (in window mode)	$25 \mu\text{s}$
Position resolution	$17 \mu\text{m}$ or better
Energy resolution (single sample)	below $5 e^-$ r.m.s.
Energy resolution (wth RDNR)	below $1 e^-$ r.m.s.
Low energy threshold	below 100 eV
Energy range above 60 % Q.E.	150 eV – 15 keV

Table 1: Summary of the DEPFET APS properties

4. FOCAL PLANE CONCEPT

Figure 7 shows a schematic layout of the WFI focal plane with three possible expansions briefly listed here. To minimize dead layer between the systems they are staggered along the focal axis.

4.1. Hard X-ray detector

The hard X-ray detector [6] is located below the APS matrix. It receives only photons which have passed through the $500 \mu\text{m}$ silicon bulk of the APS chip. The relative photon rate at 20 keV is about 60 % (40 % are still converted in the APS) and increases to more than 85 % at 30 keV. The suggested detector will probably have pixel dimensions of about $200 \mu\text{m}$ and be based on CdTe technology.

4.2. CCD Ring

In anticipation of the XEUS phase B, when the collection area shall be expanded, an additional MOS- or pn-CCD system is considered to surround the APS increasing the FOV to 15 arcmin.

4.3. Fast timing detector

Four arrays of silicon drift detectors – operated out of focus – are dedicated to highest count rate, timing observation [16]. Each array consists of e.g. 19 drift detector cells. At a count rate of 10^5 cts/s per cell the energy resolution is still better than 200 eV (at 6 keV, equivalent to a low energy threshold of ~ 0.5 keV) [16]. Count rates above 10^6 cts/s can such be reached with time resolutions of ~ 10 μ s, maintaining reasonable spectral energy resolution.

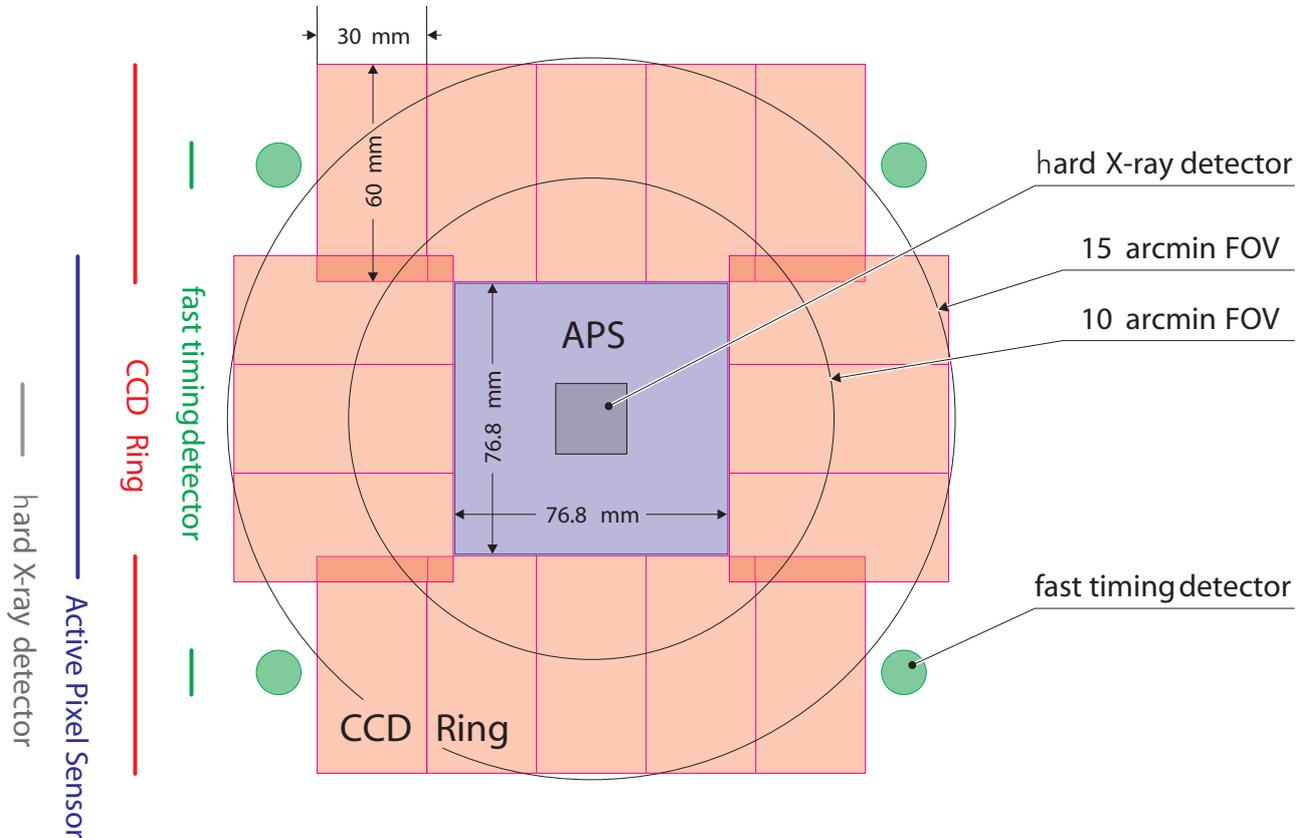


Figure 7: Focal plane layout for the XEUS WFI. The inner 5 arcmin are covered by the DEPFET APS. Three upgrade possibilities are included: the *hard X-ray detector*, *CCD Ring* and *fast timing detector*.

5. CONCLUSION

The functional principle and resulting performance make a DEPFET active pixel matrix the ideal device as the prime focal plane instruments for the WFI on XEUS. Key properties have already been verified with prototype and test devices. A current production at the MPI Halbleiterlabor includes prototypes of 64×64 pixels matrixes, p-channel and n-channel devices in circular and linear geometry. DEPFET pixels for high energy physics experiments are also included in the production. Currently about 50 % of the production steps have been completed. First measurement results are expected for early 2003.

6. REFERENCES

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