A Fast Readout for a DEPFET-Pixel Based Vertex Detector for TESLA

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A silicon detector integrating a first amplifying transistor in each pixel (DEPFET) is one promising approach for the pixel based vertex detector at TESLA. The DEPFET offers a good spatial resolution, an excellent signal to noise ratio and a low power operation mode. A readout concept for a DEPFET pixel array facing the requirements at TESLA is described. In order to meet the operation of the DEPFET device a readout architecture based on current mode techniques is presented. It performs a stand alone zero suppression offering a triggerless operation for TESLA. The core of the readout chip, a fast operating current memory cell is discussed in detail. The results of a first prototype chip show that the requirements for TESLA are achievable.

Keywords: readout electronics, Switched Current, Linear Collider, TESLA, Active Pixel Sensor, DEPFET

1. Introduction

One of the most important aims to be addressed by the detectors of a future Linear Collider like TESLA are an excellent efficiency and purity in flavor identification of hadronic jets. The separation between b and c decay tracks and the distinction between their primary, secondary and tertiary vertices should become possible. The required impact parameter resolution leads to a detector scenario where the innermost layer of the vertex detector is placed as close as possible to the interaction point. In the present design of TESLA the first layer of the vertex detector is situated at $r = 15$ mm [6]. Due to the extremely focussed beam and the high bunch charge the e^+e^--background induced by beamstrahlung becomes severely high in this region (0.03/0.05 hits per mm^2 and bunch crossing for $\sqrt{s} = 500/800$ GeV and a magnetic field of 4T [6]). The bunch structure with a long bunch train of 950 μs at TESLA imposes to read out the detector several times during the train in order to achieve a detector occupancy that does not compromise the track reconstruction. At present the readout of the whole vertex detector is set to 50 μs leading to an occupancy below 1%.

In order to minimize the multiple scattering contribution to the impact parameter resolution the reduction of any material in the detector area to a minimum is obligatory. This strongly requires a close attention to the cooling and therefore power consumption in the sensor area. All this disfavors a conventional hybrid pixel solution as used in the LHC-experiment where the readout electronics is mounted on top of the detector and every pixel is processed in parallel. On the other hand, a row wise readout of the detector -where the readout chips are place at the end of the sensor- imposes a row rate of 50 MHz in order meet a frame rate of 50 μs . To further reduce the amount of material in the detector area, a material budget of less than 0.1 % radiation length per layer is envisaged, the sensor itself is going to be thinned down to $\sim$ 50 μm. Consequently the significant reduction of the resulting signal demands a low noise detector and readout to keep a sufficient signal to noise ratio. Furthermore the sensor as well as the readout electronic has to tolerate the radiation exposure at TESLA.

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2. DEPFET Concept for TESLA

A DEPFET based pixel detector is one promising approach for the vertex detector at TESLA. The concept of the DEPFET [1] is the integration of a first amplifying transistor (junction or MOSFET) in each pixel. By means of sidewards depletion and additional implants the potential distribution in the detector is shaped in a way that a potential minimum for electrons, called the internal gate, is created right underneath the transistor channel. Electrons generated by a passing particle are accumulated in the internal gate and modulate the transistor current. A particle can therefore be detected by a changed transistor current. The external gate of each transistor can be used to switch on the amplifying transistor in order to probe the device current. Note that for the mere accumulation of charge itself the transistor does not need to be switched on. Due to the non-destructive readout of the pixel device the charge in the internal gate has to be removed from time to time. This reset procedure is also called clear and is realized by an extra contact at the border area of each pixel. Such DEPFET devices have already been produced demonstrating a very low noise performance of less than 5 e^- rms with single devices [3]. Currently manufactured DEPFET devices are designed to achieve a gain of up to 1 nA per electron collected in the internal gate.

Several DEPFET devices can be arranged in an array (see upper part of Fig. 3) to cover a large sensor area. The external gate contacts as well as the clear contacts of each row are merged. The drains of the amplifying transistors providing the device current are connected column wise. A readout chip placed at the column bottom processes the signals of this row if only one specific row is selected by switching off the rest of the transistors in the array, . This way of controlling a DEPFET array has already been successfully used in the BIOSCOPE-System [2] designed for biomedical applications. The conceptual design of a DEPFET-based ladder for TESLA is shown in Fig. 1. The sensor area itself is thinned down to ~ 50 μm leaving a thicker frame for mechanical stability. Steering chips for row selection and

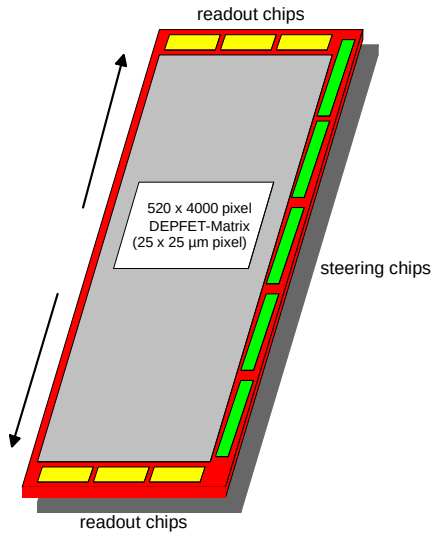

Figure 1. Conceptual design of one ladder of layer 1 of the DEPFET based vertex detector for TESLA.

reset as well as readout chips are placed onto the frame. The steering chips at the ladder side and the readout chips outside the sensor area at the ladder end. The readout of the sensor is done in both directions improving the readout speed by a factor of 2. For the vertex detector of a future linear collider the DEPFET offers:

- a small possible pixel size (20-30 μm) leading to a high spatial resolution
- an excellent signal to noise even at room temperature due to the integrated amplification
- a low power operation is performed because most of the transistors of a matrix are switched off while accumulating charge and only consume power during read out.

To meet the features of the DEPFET sensor a fast readout with still moderate noise performance has to be developed. The design concept and realization of such a readout chip will be subject of the following sections.

3. Architecture of the Readout Chip

The basic architecture of the readout chip is presented in Fig. 2. As the signal of the DEPFET device is a current and a fast readout is needed the architecture is completely based on current mode signal processing. In the first part of the chip a regulated cascode keeps the potential of the input node constant eliminating the influence of the large sensor capacitance and the effect of the limited output conductance of the pixel transistor itself. After a DEPFET row in the array has been selected for readout the DEPFET current is stored in a current memory cell. The same row is then reset and the remaining pedestal is subtracted from the buffered current automatically at the output node of the memory cell due to its inverting property. The so derived signal current is stored in a FIFO like analog memory structure. This procedure guarantees a continuous readout of the sensor with a constant readout speed independently of the occupancy. As the two measurements of the signal and pedestal are performed shortly after each other the 1/f noise of the system can intrinsically be reduced. Furthermore is noise originated by leakage current in the sensor reduced by the short frame time that is used.

In the second part of the chip the FIFO structure is emptied successively. Immediately after storing the currents in a FIFO row a parallel current compare for each column generates a digital hit pattern indicating signals above the threshold (hits). If there is no hit found in the complete FIFO row or if the amount of hits exceeds a programable maximum value the row is skipped and overwritten by succeeding cycles. According to the digital hit pattern all analog cells in the row containing no hits are turned off in order to save static power. A digital hit finder [7] identifies the hits in the digital pattern of a row and multiplexes the corresponding analog values to an algorithmic ADC. The hit finder finds up to 2 hits per cycle and processes a row until no more hits are found. The FIFO row is then available again for new data. Note that the FIFO structure's purpose is to derandomize the number of hits occurring in the sensor rows. Therefore a constant readout

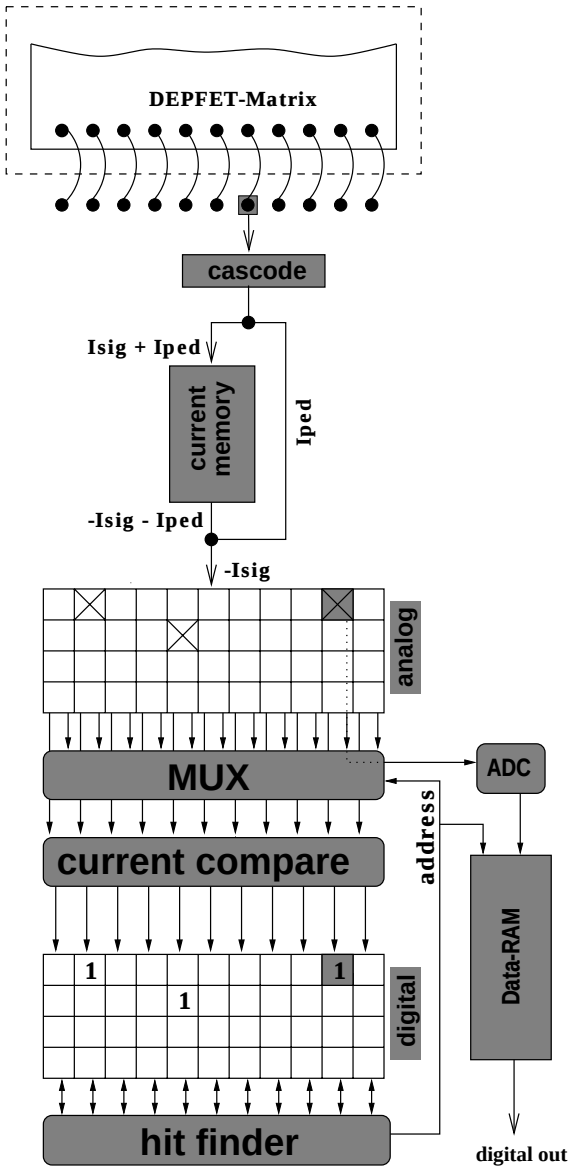

Figure 2. Basic Architecture of the readout chip. Partially only one channel is shown for simplicity.

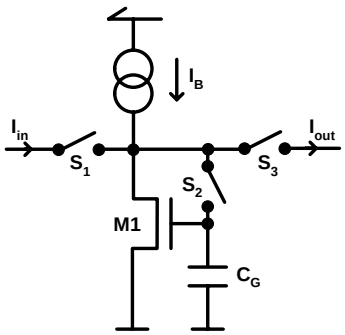

Figure 3. Basic principle of the current memory stage.

rate performed by the hit finder and the ADC can be used to read out the sensor. It is essential that the average hit occupancy does not exceed the readout rate of the hit finder. For the occupancy occurring at TESLA one hit finder will be sufficient. To cope with larger occupancies more hit finders can be used in parallel. The maximum number of hits to be allowed in a row before it is skipped by the algorithm can be influenced by the FIFO depth of course. Anyhow it is advantageous to set a limit on the maximal permitted occupancy in a row because a overfull row compromises the whole readout and additionally may not be physically interesting.

Due to the immense data reduction only one fast ADC or several low speed ADCs are needed improving the power consumption of the readout chip. After the analog to digital conversion the hit value and its address are stored in a RAM for later readout. As the readout architecture offers a stand alone hit detection no hardware trigger is needed at all.

4. Analysis of the Current Memory Cell

The most challenging part of the readout architecture in section 3 is the fast and precise buffering of the DEPFET-current for the pedestal subtraction and the storage in the analog FIFO. The design of such a current memory cell is described in this section. The basic principle of a current memory stage [4] is shown in Fig. 3 where C_G is the parasitic gate capacitance of the transistor M1. The sample and hold process is divided into three phases.

1. Only switches S1 and S2 are closed and the gate capacitance of the transistor M1 is charged until the device provides the combined input and bias current.

2. Switch S2 is opened and the gate voltage and therefore the transistor current ideally remains unchanged.

3. Right after the sampling phase switch S1 can be opened and S3 closed in order to deliver the inverted input current to the output.

Thus in the ideal case $I_{out} = -I_{in}$. However this simple circuit suffers from several non-ideal effects like charge-injection of the sampling switch S2 and the limited output conductance of the transistor M1 and the biasing current source. Therefore in the real case $I_{out} = -I_{in} + \delta I$ where δI indicates the error made by the sampling process. A lot of techniques to compete with these deficiencies have been treated in literature. In this design cascode techniques have been used for the sampling transistor and the current source to decrease the output conductance. Other limitations and their treatment are described in the following.

4.1. Linearity of the current memory cell

The influence of charge injection of the sampling switch is inherent in any sampling system. The contribution of charge injection to an error of the sampled output current can be divided into a constant offset and a signal depending part: $\delta I = \delta I^{const} + \delta I^{sig}$. In the discussed readout architecture in section 3 the constant offset becomes non-relevant because it can be compensated by an adjusted threshold in the current compare. But the signal depending charge injection will cause a nonlinearity in the transfer function of the memory cell and should therefore be reduced to a minimum.

To reduce the signal depending charge injection the circuit in Fig. 4 is used. The sampling process is divided into 2 steps realized by two successive memory stages, a coarse and a fine one. At any time switches S2 and S3 as well as

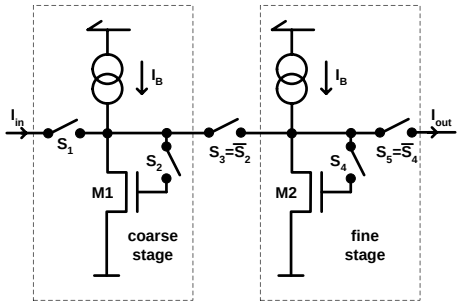

Figure 4. Basic principle of the two stage current memory cell.

switches S4 and S5 are driven complementary as indicated in the figure. The initial state of the switches are: S1, S2 and S4 closed. After the first sampling step (S2 is opened) the resulting current through M1 is $I_{M1} = I_{in} + I_{Bias} - \delta I_c$ where $\delta I_c = \delta I_c^{const} + \delta I_c^{sig}$ indicates the total error (including charge injection) made by the coarse stage. As the input current is still connected to the circuit the resulting output current of the coarse stage is δI_c which becomes the input current of the succeeding fine stage. After the second sampling step (S4 is opened) the current through M2 is $I_{M2} = \delta I_c + I_{Bias} - \delta I_f$ where $\delta I_f = \delta I_f^{const} + \delta I_f^{sig}$ is the fine stage's error. Finally the input switch S1 is opened resulting to an output current $I_{out} = -I_{in} + \delta I_f$.

The error of the coarse stage δI_c does therefore no longer contribute to the sampled output. Even though the constant parts of the errors δI_c and δI_f are similar their signal depending parts are different because the input range of the fine stage δI_c is much smaller than the input range of the coarse stage I_{in}. Since the signal depending part of charge injection causes the nonlinearity of the cell it can be reduced by an order of magnitude by the double stage sampling.

Due to the inverting feature of the memory cell itself a total cancellation of charge injection can be achieved if two successive memory cells are used like in the proposed readout architecture in section 3 (The first for the pedestal subtraction and the second in the FIFO memory). The output current of this package is $I_{out} = -(-I_{in} + \delta I_{f1}) + \delta I_{f2}$. Assuming that the charge injection of both fine stages are the same

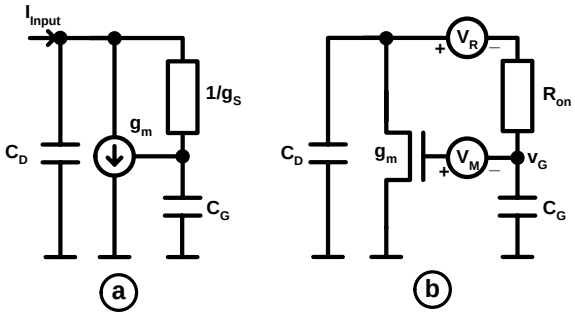

Figure 5. Equivalent circuit of the current memory cell during the charging phase (a), Circuit used for the noise analysis (b).

($\delta I_{f1} = \delta I_{f2}$) a total cancellation of charge injection is reached. This is likely because the charge injection of the fine stages are dominated by the constant fraction and not by the signal depending part and should therefore be similar. However a total cancellation is not crucial for the readout architecture as mentioned before.

4.2. Settling behavior

For a high speed application the settling behavior of the circuit has to be considered as well. During the sampling process a sufficient time is required to charge the gate capacitance of the storage transistor. Otherwise the residual voltage difference will cause a settling error in the sampled output. Fig. 5a shows the small signal equivalent circuit of the current memory cell during the charging phase. C_D is the capacitive load of the input node (usually dominated by a bus capacitance), $\frac{1}{g_s}$ the on-resistance of the sampling switch and g_m the transconductance of the memory transistor. The transfer function of this circuit is of second order:

$$H(s) = \left(1 + s\frac{C_D + C_G}{g_m} + s^2\frac{C_G C_D}{g_m g_s}\right)^{-1} \qquad (1)$$

The influence of the memory transistor channel resistance has been neglected as it is greatly reduced by the cascode. Depending on $Q = \frac{\sqrt{\frac{g_m}{g_s} C_D C_G}}{C_D + C_G}$ the time response of the circuit can either be overdamped ($Q < 0.5$), underdamped ($Q > 0.5$) or critically damped ($Q = 0.5$). Even if the fastest settling time can be achieved with the underdamped case the parameters in the de-

sign were chosen to perform the overdamped case in order to avoid oscillation in the circuit.

Contrary to a conventional voltage sampling circuit the charging time does not only depend on the switch resistance g_s and the capacitive load (C_G and C_D) but also on the g_m of the storage transistor. Therefore an improved settling time can be obtained by a high transistor g_m keeping a large storage capacitance for high accuracy. Of course this scenario is limited by the transistor geometry which links g_m and C_G together. For the two stage sampling process mentioned in section 4.1 two settling times have to be considered. However, t_{fine} can be chosen much larger than t_{coarse} as the error of the coarse stage does not contribute to the output directly .

4.3. Noise Analysis

Another limitation of the current memory cell's performance is the sampling noise. It is originated by a variation of the gate voltage of the memory transistor during the sampling phase caused by different noise sources in the circuit. At the end of the sampling phase the noise voltage is stored at the gate capacitance and results in a current noise at the output. Fig. 5b shows the different noise sources considered in this analysis. The transistor noise itself is modelled by the voltage source V_M and the noise contribution of the switch resistance is given by V_R. For several reasons this analysis can focus on thermal noise consideration. First large area transistors (A$\sim$100 μm) were used for sampling, secondly does the wide bandwidth of the circuit emphasize the thermal noise contribution and finally 1/f noise is suppressed by the inherent correlated double sampled performed by the memory cell [8]. Therefore a white noise spectrum is assumed for the noise sources modelled by $\langle V_R^2 \rangle = 4kTR_{on}$ for the switch resistance and $\langle V_M^2 \rangle = \frac{8}{3}kTg_m^{-1}$ for the sampling transistor itself. Calculating the amplitude of the filtered gate voltage leads to a total rms noise for the output current of

$$\langle i_{out}^2 \rangle = g_m^2 \langle v_G^2 \rangle = g_m^2 \frac{kT}{C_G} \left(\frac{\frac{2}{3}C_G + C_D}{C_G + C_D} \right). \qquad (2)$$

Like in a voltage sample and hold the switch resistance R_{on} does not influence the sampling noise.

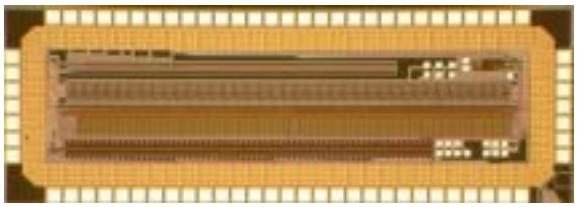

Figure 6. Photography of the 1.5x4 mm^2 prototype chip in 0.25 μm radiation tolerant CMOS technology.

For all possible drain and gate capacitances the bracket in (2) is a factor between $\frac{2}{3}$ and 1. Neglecting the bracket the sampling noise becomes approximately $\langle i_{out}^2 \rangle \approx g_m^2 \frac{kT}{C_G}$ and is therefore almost independent of C_D. With the design parameters $g_m \approx 370$ μS and $C_G \approx 620$ fF a sampling noise of 24 nA ... 30 nA (depending on the drain capacitance) is expected. Note that even in the case of the double staged cell mentioned in section 4.1 the sampling noise is still given by (2) because the error (including the sampling noise) of the coarse stage is corrected by the fine stage. The noise contribution of the biasing current source has been neglected in this calculation. It can be simply added to the sampling noise if it becomes considerably high.

5. Results

A first prototype chip implementing all major building blocks described in section 3 has been manufactured using a 5 metal 0.25 μm CMOS technology with a radiation tolerant design. Note that the radiation tolerant layout imposes several constraints on the transistor parameters [5]. Fig. 6 shows a photography of the 1.5x4 mm^2 prototype chip. The current comparator and the digital hit finder have been successfully tested up to 50 MHz.

The measured linearity of the analog front-end consisting of 2 successive current memory cells with the regulated input cascode is given in Fig. 7. The linearity decreases for currents larger than 50 μA as the input comes into the range of the bias current used in the cell. Therefore a tradeoff between static power consumption and dynamic range has to be made. For a DEPFET readout a

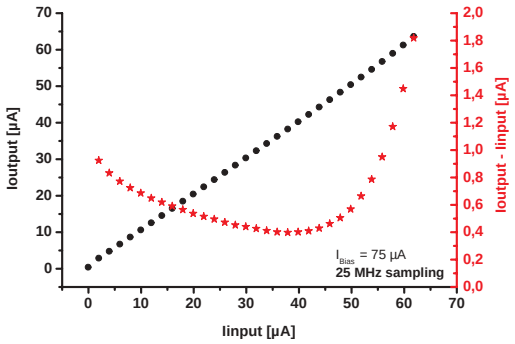

Figure 7. Linearity of the complete analog front-end (The points indicating the output current and the stars indicating the deviation between input and output current).

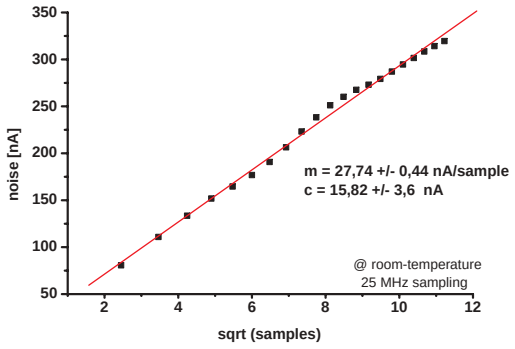

Figure 8. Total sampling noise as a function of the square root of the number of sampling steps.

dynamic range of about 10 μA (equivalent 10000 electrons) is sufficient. Fig. 7 shows an accuracy of the complete analog stage for the required dynamic range of better than 0.1% at 25 MHz sampling frequency.

To analyze the noise contribution of the memory cell a queue of several successive cells has been implemented. Therefore the number of samples that are made before the output current is measured can be varied over a large range. Fig. 8 shows the measured total noise at the output depending on the number of sampling steps. As shown in Fig. 8 do independent noise contributions add quadratically and the total noise of the sampling chain has a linear dependency on the square root of the number of sampling steps. A linear fit extracts a sampling noise of less than 28 nA (ENC=28 e^-) per sample which corresponds to the calculated value in section 4.3. This shows that the noise of the current memory cell is mainly given by the thermal noise contributions of the sampling process as assumed in the noise analysis.

6. Conclusion

A readout concept for a DEPFET pixel based vertex detector facing the requirements at TESLA has been developed. The proposed readout concept is completely based on current mode techniques joining the current operation mode of the DEPFET sensor. The architecture of the readout chip offers correlated double sampling of the input signal and a triggerless zero suppression. The results of a first prototype chip using a radiation tolerant design show that the requirements are achievable. A full readout chip for a DEPFET array is being designed at present.

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