Processing of Ultra-Thin Silicon Sensors for Future e⁺e⁻ Linear Collider Experiments

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Abstract--**The e⁺e⁻ linear collider physics program sets highly demanding requirements on the accurate determination of charged particle trajectories close to the interaction point. A new generation of DEPFET active pixel sensors with 25 μm pixel size is currently being developed to meet the requirements in the point measurement resolution and multiple track separation. To minimize the influence of the multiple scattering on the impact parameter resolution, the sensors have to be made as thin as possible. The paper presents a technology based on direct wafer bonding and deep anisotropic etching for the production of ultra-thin fully depleted sensors with electrically active back side. PiN diodes with 50 μm thickness have been produced in this way and the results show the feasibility of this approach. The technology is useful for the production of any kind of thin sensors with active back side (strip detectors, pad detectors etc.). An integrated support frame outside the sensitive area allows for safe handling and mounting of the thin devices.**

I. INTRODUCTION

The vertex detector for a future linear e⁺e⁻ collider (e.g. TESLA) will be a set of cylindrical detectors arranged in ladders around the interaction point[1]. Each ladder is an array of pixel cells read out at the end of the ladder outside the fiducial volume. The figure of merit for such a detector is the resolution in the impact parameter σ_IP which can be expressed as

$$\sigma_{IP} = \sqrt{a^2 + \left(\frac{b}{p \cdot \sin^{3/2} \Theta}\right)^2} \qquad (1)$$

The constant *a* accounts for the point resolution and geometrical stability of the detectors and the second term with the constant *b* represents the resolution degradation due to multiple scattering. This second term depends on the track momentum *p* and the polar angle Θ. The support structure for the sensor module, cooling pipes for active cooling of the sensor, and the sensor material itself contribute to the material budget and degrade the detector performance. In the case of a DEPFET (DEPleted Field Effect Transistor) as the pixel cell, the signal charge is measured in every pixel on a row-by-row basis and the DEPFETs are successively switched on by means of gating lines. A detailed description of the read-out scheme and the DEPFET sensor itself can be found in [2] and [3]. The row-wise read out minimizes the power consumption in the sensitive area and therefore the effort and material needed for cooling.

This paper presents our approach to minimize the contributions of the support structure and sensor material to the material budget of the vertex detector. The technology is developed for DEPFET pixel sensors for future linear collider experiments but it is applicable to any kind of silicon radiation sensors with electrically active backside.

II. MODULE CONCEPT FOR THIN DEPFET PIXEL ARRAYS

In our concept the DEPFET pixel array is made on thin (~50 μm in this study) detector grade silicon supported by a directly bonded silicon frame of ~300 μm thickness. The dimensions of the sensitive area in the first layer of the vertex detector at TESLA are 100x13 mm². The read-out electronics, the lines for power, slow control, and data transmission are placed at both short sides of the ladder outside the fiducial volume of the vertex detector; the thinned steering chips (also ~50 μm) for the row-wise read out are attached on the thick frame along the long side of the ladder. The circuit paths for these steering chips are integrated on the support frame of the sensor module. Ideally, although not essential, the circuit paths of the front-end electronics, control logic, and data transmission drivers located the ends of the ladder are made in the same way. The read-out circuits at the ends are attached to cooling blocks outside the fiducial volume of the vertex detector. Fig. 1 shows the sketch of a module for the first layer of the TESLA vertex detector.
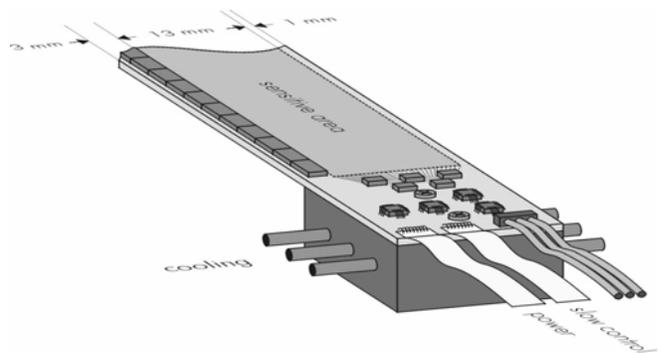

Fig. 1. Sketch of a TESLA first layer module with thinned sensitive area supported by a silicon frame.

The biggest contribution to the material budget would be a massive support frame along the long sides. In the proposed technology it is possible to etch cavities in the supporting silicon forming a support grid instead of a massive frame. Fig. 2 shows a mechanical sample which illustrates the concept. The mirror like surface in the center of the sample is the back side of the thinned active sensor area; the surrounding surface is the supporting thick frame with the 250 μm deep cavities for further material reduction. The material contribution of such a module for the first barrel of the TESLA vertex detector is 0.11 % of a radiation length X_0, including the frame and the (also back thinned) steering chips at the edge.
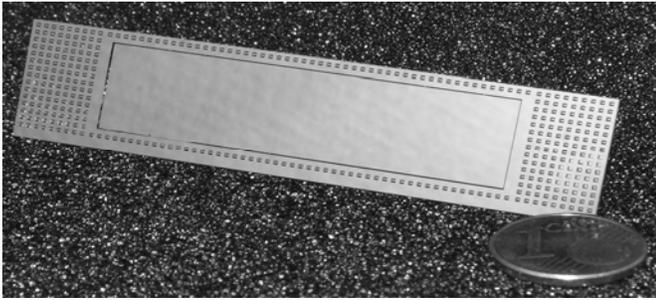

Fig. 2. The mirror like surface in the center of the mechanical sample is the back side of the 50 μm thin active sensor area surrounded by a supporting 300 μm thick frame with 250 μm deep cavities for material reduction.

III. TECHNOLOGY

Back thinning of microelectronic chips is already widely used in semiconductor industry. However, these technologies are not applicable for fully depleted sensors with an electrically active backside. FETs on fully depleted bulk with a deep-n implant under the channel (DEPFETs) combine charge generation and first amplification in one single device. They have a structured implant, contacts, and metallization at the back side. Fig. 3 shows the principle of such a device. Conventional thinning, i.e. chemical mechanical polishing (CMP) of the back side, is usually done after the top side processing is finished. The processing steps at the back side had then to be done with a thin and fragile wafer, a procedure which is obviously extremely difficult and cost-intensive.
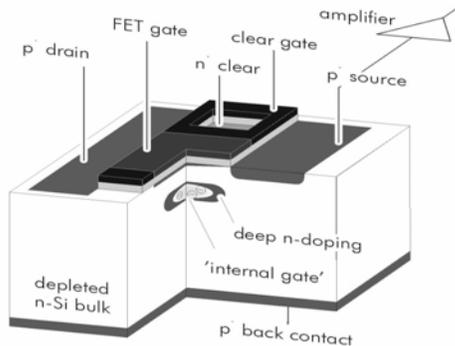

Fig. 3. Cross-section of a DEPFET (DEPleted Field Effect Transistor). Electron-hole pairs generated by penetrating radiation are separated in the depleted bulk. The electrons are stored in the potential maximum ('internal gate') under the channel of an FET and modulate the source-drain current.

Fig. 4 illustrates our approach to build such thin devices with a minimum of processing steps after thinning. The process sequence starts with two oxidized silicon wafers. The top wafer will be the thin device wafer with the DEPFET matrix; the second one is the handle wafer which will later form the supporting frame. The back side implantation for the DEPFETs is already done at this stage of the processing (Fig.4a).

These two wafers are then bonded directly to each other using a wafer bonding technique described in [4], forming a stack of two wafers with buried back side implants for the top wafer devices and silicon oxide in between. After a high temperature annealing (>1000ºC) the cohesion between the two wafers is due to Si-O-Si bonds and the stack cannot be separated without breaking the wafer. The top wafer is then thinned to the desired thickness of the sensor matrix using conventional equipment for wafer grinding and polishing (Fig.4b).
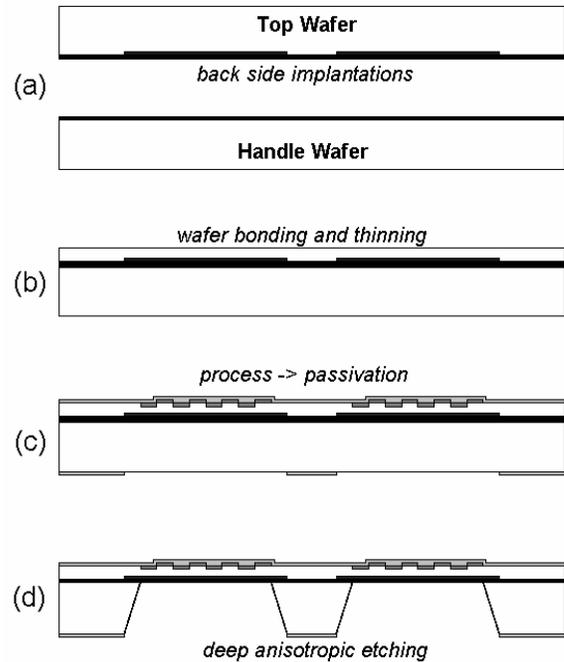

Fig. 4. The process sequence for production of thin silicon sensors with electrically active back side implant starts with the oxidation of the top and handle wafer and the back side implantation for the sensor devices(a). After direct wafer bonding, the top wafer is thinned and polished to the desired thickness(b). The processing of the devices on the top side of the wafer stack is done on conventional equipment; the openings in the back side passivation define the areas where the bulk of the handle wafer will be removed(c). The bulk of the handle wafer is removed by deep anisotropic wet etching. The etch process stops at the silicon oxide interface between the two wafers(d).

The thermal and mechanical stability of this wafer stack is almost like for a conventional wafer and all subsequent

process steps needed for microelectronic production can be done with the usual equipment for semiconductor manufacturing (Fig.4c). Another advantage of this technology is that the sensitive back side of the sensor wafer is now covered by the handle wafer and no special precautions are needed to protect the back side during top wafer processing. The last step of the top side processing is the deposition and patterning of the passivation layer, leaving only the aluminium bond pads of the sensor uncovered.

The back side passivation under the sensitive area of the sensor is removed and the silicon of the handle wafer is selectively etched away (Fig.4d). The passivation layer protects the top wafer and serves as the etch mask for the deep etching of the handle wafer from the back side. The etch solution is tetramethyl ammonium hydroxide (TMAH). This organic alkaline solution is an anisotropic etchant for mono-crystalline silicon with a much higher etch rate for the (100) plane than for the (111) plane. In contrast to KOH (potassium hydroxide), TMAH contains no alkali ions and has an excellent selectivity to SiO_2 and Si_3N_4 (the commonly used passivation layers) but in its pure form it attacks the aluminium of the bond pads. The aluminium etch rate can be significantly reduced by dissolving silicon in TMAH and adding ammonium peroxodisulfate $((NH_4)_2S_2O_8)$ to maintain a high silicon etch rate[5]. The formulation proposed in [5] is 5 wt.% TMAH, 1.6 wt.% dissolved silicon, and 0.5 wt.% $((NH_4)_2S_2O_8)$. At 85°C we achieved with this solution an etch rate of ~35 μm/h for the silicon (100) plane without any measurable effect on SiO_2 and aluminium. The etch process stops after 7 to 9 hours when the handle wafer is etched through and the etch solution reaches the buried SiO_2 layer between the top and the handle wafer. The back side implant and the sensitive bulk of the sensor are not affected by the etching process.
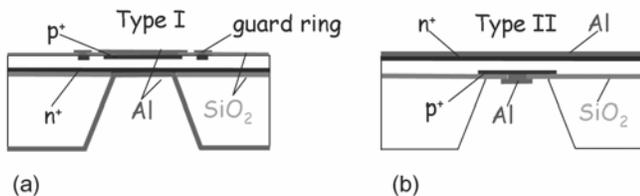

Fig. 5. Cross-sections of the two different types of PiN diodes on high resistivity n⁻-substrate. Type I has a large-area area ohmic contact at the bond interface with pn-junctions and guard rings at the top wafer surface(a), Type II is vice versa with a structured p⁺-implant at the bond interface and a large-area ohmic contact at the top wafer surface(b).

In the case of a rectifying implant at the back side of the top wafer (Fig. 5b), there are still two lithographic steps (i.e. contact opening in the buried oxide and patterning of the metallization) needed to keep the bulk of the handle wafer isolated from back side implant at the top wafer. However, the requirements on the accuracy are here extremely relaxed and can easily be met even on the extreme topography of the etched back side. Due to the integrated support frames, the handling of the wafer is relatively safe even at this stage of the processing. There are no further lithography steps needed for devices with an ohmic back side contact. These devices are ready for dicing after the large-area back side metallization.

Direct wafer bonding and thinning of the top wafer is widely used for production of SOI (Silicon on Insulator) wafers and anisotropic deep etching is a standard procedure to build membranes and cantilevers for MEMS (Micro-Electro-Mechanical Systems) devices such as accelerometers or pressure sensors (see e.g. [4] and references therein). The challenge in our application is the integration of these individual steps into a process sequence for production of fully depleted silicon sensors.

IV. ULTRA-THIN PiN DIODES

In order to investigate whether this technology is feasible and how it affects the basic characteristics of the thin devices, two types of 50 μm thin PiN diodes on high resistivity phosphorous doped silicon substrate have been made (Fig. 5).

Test devices of the type I are 10 mm² diodes with structured p⁺-implant and guard ring at the top wafer surface. The large-area n⁺-implant is in the bond region between the two wafers. The back side contact is made with a large-area aluminium metallization (see Fig. 5a).
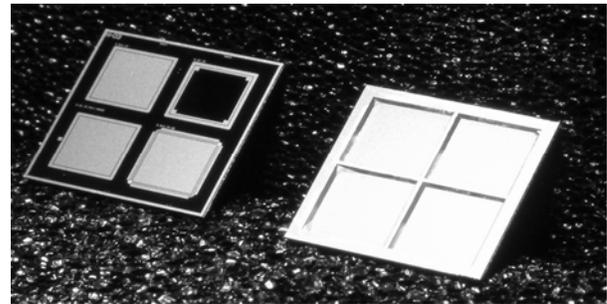

Fig. 6. Top (left) and handle wafer side (right) of two diced chips (1 cm²) with four 10 mm² diodes of the Type I on 50 μm thin silicon.

Fig. 6 shows the front and back side of diced chips, each of them with four diodes of Type I in the thin windows. The diodes of Type II are the other way around: unstructured n⁺ on the top wafer, structured p⁺ in the bond region (see Fig. 5b). The aim of Type I was to have a direct comparison of the reverse current of thin diodes with standard diodes on thick material produced in the same way, except for the wafer bonding and etching. The diodes of the type II were made mainly to test for bondability of the wafers after lithography and implantation at the bond interface.

Fig. 7 shows a typical $1/C^2(V)$-curve of a Type I diode, C being the capacitance of the pn-junction and V the reverse bias. As expected, the curve is linear below full depletion and goes into saturation above. The full depletion voltage for this wafer is 2.5 V. The thickness of the substrate, extracted from the absolute value of the capacitance at high voltages, is 47 μm. The calculated resistivity of the substrate is then about

3 kΩ·cm, which is inside the range specified by the vendor of the substrates.

Fig. 8 shows typical bulk generated currents of three Type I diodes as a function of the applied reverse bias voltage. There was no breakdown observed even at strong over-depletion of the diodes. The reverse current per unit volume is about 150 nA/cm^3 at 5 V bias voltage, both before and after etching of the handle wafer. In the former case the electrical contact to the back side was made over the edge of the wafer stack. The reverse current per unit volume of the thin diodes is four times higher than the one of the reference diodes of the same type, processed on the same equipment but with 250 μm thickness.
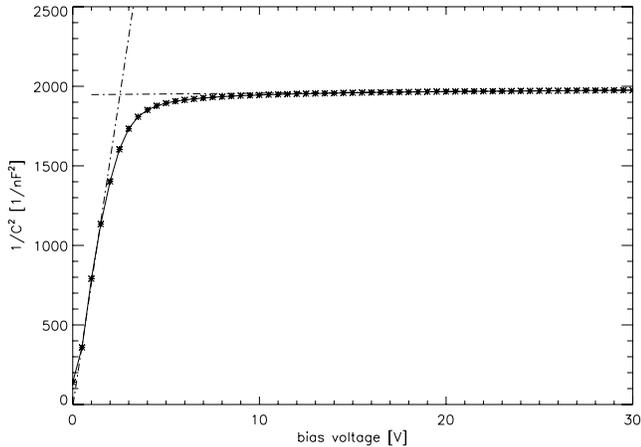
The IV-curves of the diodes of type II, with the structured p+ in the bond region, have similar characteristics. Fig. 9 shows the reverse currents at 5 V bias versus the area of these diodes. In contrast to the diodes of the type I, with this type it is not possible to separate the bulk and the edge generated current. The contribution of the edge to the total measured reverse current is seen in the fact that the measured current does not scale with the area of the pn-junction. Nevertheless, the biggest diodes of the type II (6.5 cm^2) have with 123 nA/cm^3 at 5 V bias an even lower total reverse current compared with the thin diodes of type I.

Fig. 7. The capacitance of a Type I diode as function of the reverse bias, drawn in the form 1/C^2(V). The intercept of the two linear fits indicates a full depletion of 2.5 V. The thickness calculated from the measured capacitance at high reverse bias is 47 μm.

Fig. 9. Currents at 5 V a reverse bias versus the area of thin Type II PiN diodes with different sizes ranging from 0.09 cm^2 to 6.5 cm^2.

This difference can be attributed to the stress and possibly contamination during the bonding procedure and the different thermal budget of the thin diodes due to the high temperature annealing after direct wafer bonding. This is now subject of further investigations and optimizations. However, even without these optimizations, the reverse currents of the thin diodes are at an entirely acceptable level for semiconductor tracking detectors.
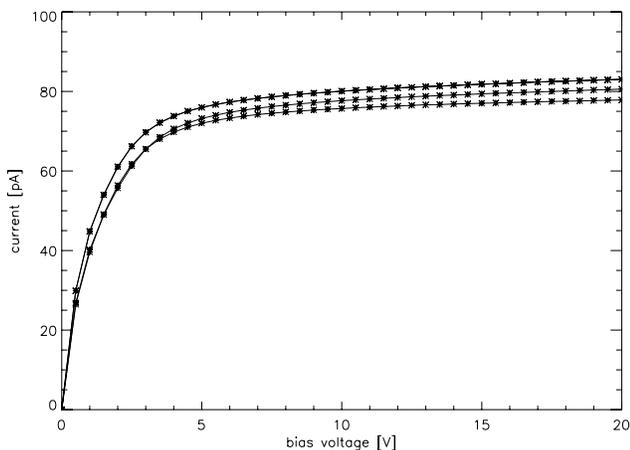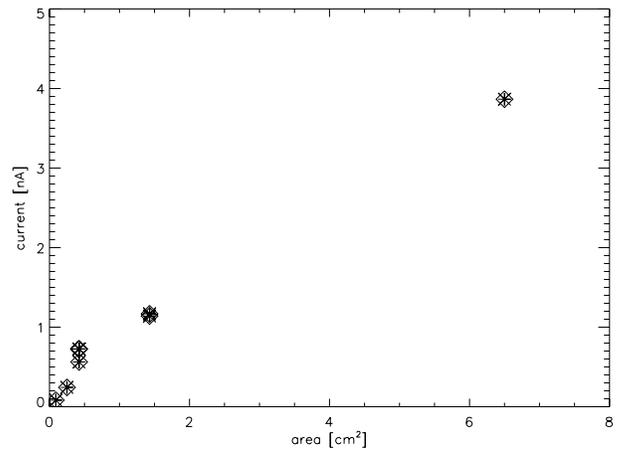

V. CONCLUSIONS

A technology based on direct wafer bonding and deep anisotropic etching for production of ultra-thin radiation detectors with electrically active back side was presented. The development was done for DEPFET arrays for the vertex detector at TESLA but it is applicable for all kinds of sensors with active back side (strip detectors, pad detectors etc.). A technology test run with various PiN diodes showed the feasibility of the technology. Direct wafer bonding is possible even after lithography and implantation at the bond interface of the top wafer. The deep anisotropic etching of the handle wafer does not deteriorate the characteristics of the PiN diodes and the handling of the etched wafers and diced thin chips with the integrated support frame is safe and easy.

There are some indications that the processes of wafer bonding and the subsequent high temperature annealing adversely affect the reverse current of the PiN diodes. However, the level achieved in this first test is already perfectly suitable for semiconductor tracking detectors.

The results achieved so far encourage the production of thin DEPFET pixel arrays with this technology.

VI. REFERENCES

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