First results from electrical qualification measurements on DEPFET pixel detectors

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ABSTRACT

We report on the first results from a new setup for electrical qualification measurements of DEPFET pixel detector matrices. In order to measure the transistor properties of all pixels, the DEPFET device is placed into a benchtest setup and electrically contacted via a probecard. Using a switch matrix, each pixel of the detector array can be addressed individually for characterization.
These measurements facilitate to pre-select the best DEPFET matrices as detector device prior to the mounting of the matrix and allow to investigate topics like the homogeneity of transistor parameters on device, wafer and batch level in order to learn about the stability and reproducibility of the production process. Especially with regard to the detector development for the IXO Wide Field Imager (WFI), this yield learning will be an important tool.
The first electrical qualification measurements with this setup were done on DEPFET macropixel detector flight hardware, which will form the FPAs of the Mercury Imaging X-ray Spectrometer (MIXS) on board of the 5th ESA cornerstone mission BepiColombo. The DEPFET array consists of 64×64 macropixel for which the transfer, output and clear characteristics were measured.

Keywords: DEPFET, Active Pixel Sensor, Electrical Characterization, BepiColombo, IXO, WFI

1. INTRODUCTION

The DEPFET detector is an active pixel device, where each individual pixel intrinsically amplifies the detected signal. The outstanding characteristics of this technology come from a combination of favorable properties, for example an excellent energy resolution, low noise readout at high speed, low power consumption and the possibility of read-out on demand.[1] A recent development is the DEPFET macropixel,[2,3] which combines the DEPFET and the Silicon Drift Detector (SDD) concept. This advance introduces the capability of easily scalable pixel size up to the cm^2 range, which allows to tailor the DEPFET pixel in order to meet the experimental requirements. Since a couple of years, detectors based on the DEPFET principle are being implemented in planned space-borne applications[1,4–6] as well as in high energy particle physics[7,8] and photon science.[9] In the following we will focus on space applications.

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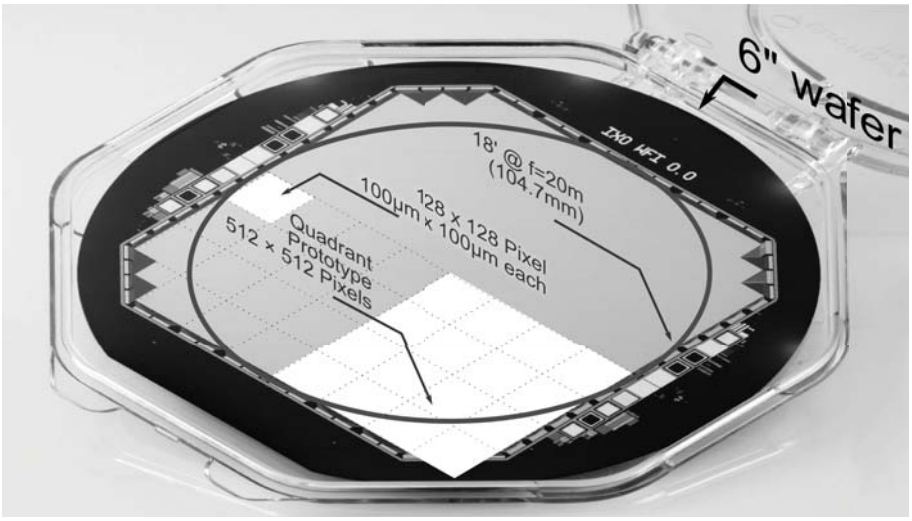

Figure 1. Mechanical prototype of the IXO WFI 6 inch wafer-scale detector. The circle depicts the 18' FOV. The logical layout of the detector is overplotted on one hemisphere. The white fields indicate the size of an array of 128x128 pixels as well as the size of the Quadrant Prototype consisting of 512×512 pixels.

The first space mission flying a DEPFET detector will be BepiColombo, the 5th cornerstone mission of the European Space Agency (ESA) in collaboration with the Japanese Space Agency (JAXA). This mission, which will be launched in 2014, is dedicated to the exploration of Mercury and equipped with a large suite of instruments.[10] One of the instruments, the Mercury Imaging X-ray Spectrometer (MIXS),[4,11,12] will investigate the element abundance of the planet's crust by measuring the characteristic X-ray fluorescence lines emitted from the surface. MIXS is sensitive to the energy range 0.5 keV $\leq$ E $\leq$ 10 keV in order to be able to monitor the iron K-line (6.4 keV) and L-line (0.71 keV). The MIXS comprises two instruments, one equipped with collimator optics for large area scans (MIXS-C), the other equipped with telescope optics (MIXS-T) to allow direct imaging of the fluorescence radiation with high spatial resolution. Both instruments will use identical DEPFET macropixel sensors as focal plane array (FPA). According to MIXS requirements, the sensitive area of the FPA is 1.92×1.92 cm^2, which is divided into an array of 64×64 pixels. The size of each individual pixel is 300×300 μm^2, which is driven by the size of the point spread function (PSF) of MIXS-T. The production of the first FPA flight devices has now been finished at the MPI Halbleiterlabor.

Currently, the most ambitious project concerning size and number of pixels is the DEPFET detector for the FPA of the Wide Field Imager (WFI) onboard of the International X-ray Observatory (IXO) whose launch is planned for 2021. This detector[6] will be a 6 inch wafer-scale monolithic device consisting of $\sim 10^6$ pixels. The pixel size is chosen to be 100×100 μm^2, which allows a 5-fold oversampling of the PSF. The purpose of the WFI is to provide images in the energy range of 0.1 keV $\leq$ E $\leq$ 15 keV with spatial, spectral and time resolution for a large field of view. Figure 1 shows a mechanical prototype of the IXO WFI illustrating the physical and logical layout of the detector. The production of WFI Quadrant Prototypes consisting of 512×512 pixels has already been started at the MPI Halbleiterlabor.

The integration of the MIXS flight devices,[13] let alone the assembly of the WFI Quadrant Prototypes to a detector system, is complex and time consuming. Therefore a new characterization step had to be implemented to the procedure between the dicing of the wafer and the mounting of the detector matrix, in order to be able to pre-select the best devices for mounting and to provide fast yield learning. Additionally the measurements make available valuable information for technology learning, e.g. they allow to monitor homogeneity on die, wafer and batch level.

For these electrical qualification measurements on die level, a dedicated measurement setup was developed. The DEPFET detector matrix is contacted by a probecard, which electrically connects the pixels to the measurement system consisting of a breakout board, a switch matrix, voltage supplies and ammeters. Due to the modular concept of the setup, it can be easily adapted to DEPFET devices with various geometry and number of pixels,

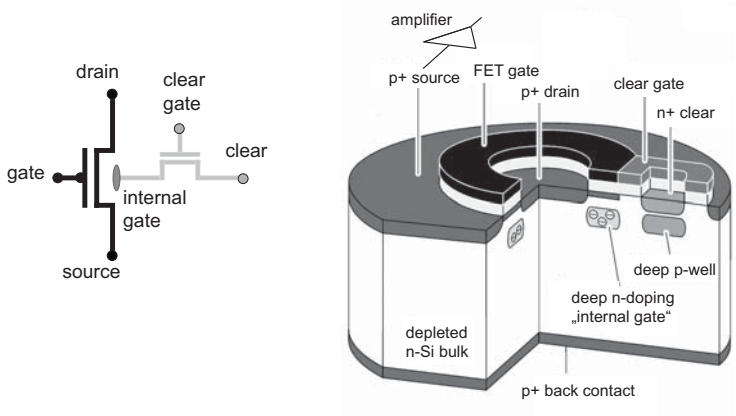

Figure 2. Schematic drawing of a circular DEPFET pixel and its equivalent circuit.[4] The pixel consists of two MOSFET structures: a circular P-channel MOSFET with an additional deep n-doping underneath the gate (*internal gate*) and an additional N-channel Clear-FET.

e.g. a change in the pixel size and the fanout of the electrical interconnections on the device only leads to a change in the probecard layout. For the WFI Quadrant Prototypes, a second switch and a new breakout board will have to be included into the setup, as the number of pixels is increased by a factor of 64 compared to the MIXS devices. While this will necessitate some software changes, the basic concept remains.
We report here on the first electrical measurements of the first batch of MIXS flight detectors, which were measured with the new DEPFET test setup at room temperature. The transfer, output and the DEPFET specific clear characteristics have been measured for each pixel and the transistor performance was compared at die, wafer and batch level.

2. THE DEPFET DETECTOR MATRIX

The DEPFET concept was first published by Kemmer and Lutz[14] in 1987 and is based on the principle of sideward depletion[15] in combination with FET structures. A schematic drawing of a DEPFET pixel is shown in figure 2. On the front side of the fully depleted, high-resistive n-doped Si bulk, two MOSFET structures are located. The main structure is a circular P-channel MOSFET with an additional deep-n doping underneath the gate, which forms a confined potential minimum. Electron-hole pairs, which are created by photons entering the detector, are separated by the high electric field. The holes drift to the backside contact and the electrons are attracted to the deep-n doped region underneath the gate. As the collected signal electrons modulate the charge carrier density in the transistor channel and alter the channel conductivity, the deep-n doped region is called *internal gate*. A second MOSFET, the N-channel Clear-FET, connects the internal gate via the *cleargate* to the n-doped *clear* region. By applying appropriate positive voltages to the clear and the cleargate, the signal electrons can be fully removed from the internal gate and the P-channel MOSFET is reset to its ground state.
The change in conductivity induced by the signal electrons in the internal gate can be used as a measure for the amount of charge collected, i.e. the energy of the absorbed photon in case of use as X-ray detector. In order to precisely measure the amount of charge collected, the method of correlated double sampling (CDS) is applied. Electrons are collected over a defined period of time and then the conductivity of the p-channel MOSFET is measured. Directly afterwards the pixel is cleared and the conductivity is measured again. The difference between both measurements can be directly attributed to the number of electrons collected during the charge integration time. For a detailed discussion of the DEPFET principle and the advantages of this technology see e.g.[2,4,16]

The pixels are organized in a matrix, where gate, clear and cleargate contacts are connected row wise. The on-chip wiring of source contacts and drain contacts is determined by the choice of front-end electronics used to readout the detector. Two complementary readout ASIC concepts are currently pursued. One of the designs, VELA,[17] is based on drain-current readout, whereas the other option, ASTEROID,[18] pursues the source-follower

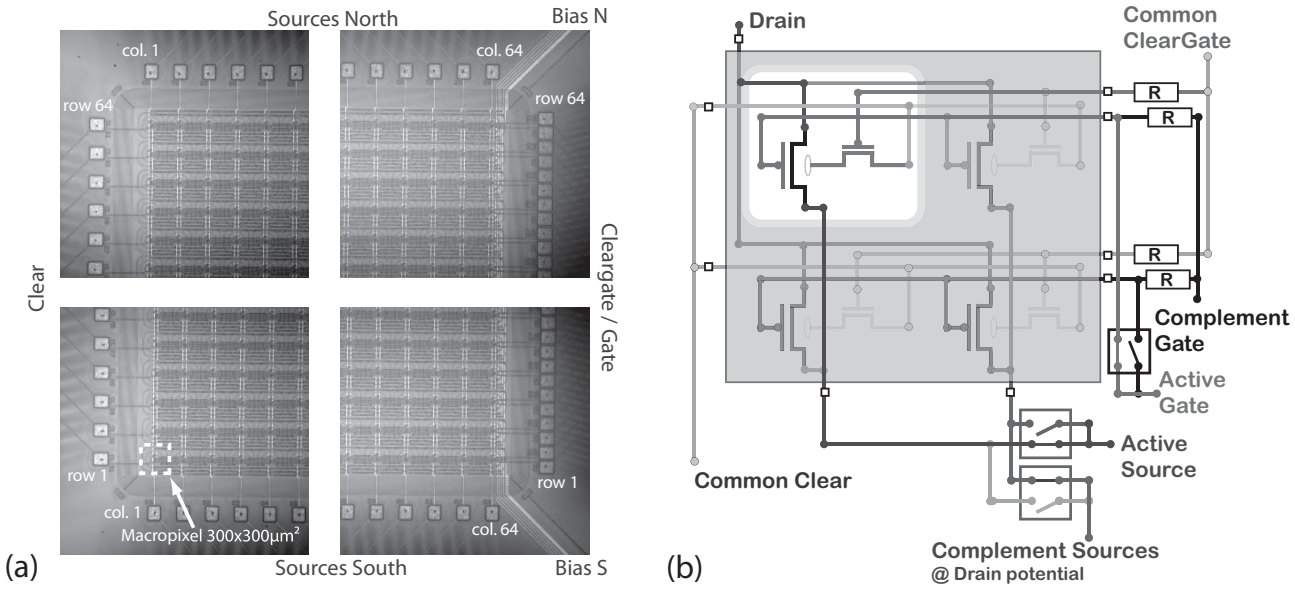

Figure 3. (a) Microphotographs of the 4 corners of a MIXS flight device. The source contacts are organized column wise and are located in the north and south. Clear, cleargate and gate contacts are organized row wise and located in the east and west. Bias North and Bias South pads are not visible, as they are located outside the main pad square.
(b) Schematic drawing of the electrical interconnections in the matrix and the configuration for benchtest measurements (see text). For the sake of clearness, a 2x2 pixel array is depicted.

configuration. For the VELA option, the drain contacts are connected column wise and the sources of all pixels are interconnected and form the source bias grid. For the ASTEROID option however, the sources are connected column wise and all drains are interconnected.
By selecting column/row pairs, each pixel can be addressed individually. When operated as a matrix, all pixels of one row are addressed simultaneously, as each column has its own readout node. The rows are adressed sequentially from the first to the last one and the collected data set of all rows is called frame. The sequence then restarts at the first row (rolling shutter mode) in order to collect the next frame. The readout time for one frame is the sum of the readout time for all rows.

The DEPFET test setup for electrical qualification measurements can cope with both readout options. For the sake of simplicity, we will limit the following discussion to the investigation of matrices designed for ASTEROID readout, as the MIXS detector devices are of this type.
The MIXS detector (64×64 pixels) has a particular layout feature, as it is electrically subdivided into a northern and a southern hemisphere, which means that each source line is connected to 32 DEPFETs instead of 64. This concept allows to readout two rows in parallel and offers a clearly enhanced frame rate at the cost of doubling the number of readout nodes. For the electrical measurements, this division is compensated at breakout board level, where each source channel from one hemisphere is connected to the appropriate source channel from the other hemisphere and therefore the standard measurement setup can be used.
Microphotographs of a MIXS flight device showing the electrical organization of the matrix is depicted in figure 3(a). The probe marks from the probecard are visible on the pads.

3. TEST SETUP FOR ELECTRICAL CHARACTERIZATION

The scope of the measurements is to investigate the characteristics of each pixel in a DEPFET matrix at room temperature. For this purpose the device is placed on a Suss PM8 manual probe station on a custom chuck adapter. By limiting the contact area of the matrix and the chuck adapter to the insensitive rim of the die, this adapter ensures that the highly sensitive entrance window on the back side of the detector matrix is not touched

during the measurements . The prober is located in a dark box to avoid parasitic currents induced by straylight. The design of the detector matrix includes probe pads in addition to bond pads, which allows to operate the matrix without touching the bond pads by using an adequate probecard. In the case of MIXS flight devices, the probecard consists of 332 needles.
Shielded flat ribbon cables connect the probecard to the breakout board where the channels are regrouped to be linked to the measurement equipment. The main instrument is a programmable Keithley 3706 switch mainframe with six Keithley 3723 Highspeed reed relay multiplexer (MUX) cards, where each MUX card provides 120 single-pole MUX channels. Furthermore a three channel Toellner power supply and a programmable Keithley 2612A two-channel SourceMeter are used. A schematic drawing of the electrical configuration is shown in figure 3(b). To select and characterize a specific pixel (column m; row n), it is mandatory that all other pixels are in a defined OFF state. To set all pixels to the OFF state, every gate channel is connected via a R = 10 kΩ series resistor to the *complement gate* potential $V_{\bar{G}} = 5$ V and all sources are connected via the *complement source MUX* to drain potential $V_{\bar{S}} = V_D$. In addition, all electrons are removed from the internal gate by connecting the cleargates - like the gates - via R = 10 kΩ series resistors to the *common cleargate* potential $V_{CG} = 5$ V and connecting the clear channels to the *common clear* potential $V_C = 10$ V. For measurements where the clear potential is static, additional R = 10 kΩ series resistors like for the other row contacts are used as well, in order to avoid voltage spikes e.g. during the power-up sequence. Access to a single pixel is provided by the *active gate MUX* and the *active source MUX*. By selecting channel n at the active gate MUX, all gates of row n are pulled to the active gate potential V_G and by opening channel m at the complement source MUX and closing the corresponding active source MUX channel, all sources of column m are set to the active source potential $V_S = 0$ V. Hence, pixel (m/n) can be characterized while all other pixels remain in the OFF state, which also avoids self-heating of the detector matrix.
The data set obtained for each pixel of a matrix comprises transfer ($I(V_G)$), output ($I(V_D)$) and clear characteristics ($I(V_C)$). In order to measure the transfer characteristics for the MIXS devices, the drain voltage is set to $V_D = -5$ V and the gate voltage is varied $V_G = 1$ V $\searrow$ -4 V, for the output characteristics the drain voltage is varied $V_D = 0$ V $\searrow$ -5.1 V for three distinct gate voltages $V_G \in [-2.7; -3.0; -3.3]$ V. The clear characteristics, which allows to study the influence of the clear voltage on the state of the internal gate and hence on the transistor current, is measured for $V_D = -5$ V, $V_G = -1$ V and $V_C = 10$ V $\searrow$ 0 V. During the measurements, all drift rings of the macropixels are biased to $V_{Ring} = -5$ V.

4. RESULTS AND DISCUSSION

All six MIXS flight matrices from the first batch are now analysed using the DEPFET test setup described in section 3. The matrices were produced on three wafers with two MIXS matrices per wafer. We found that out of the six matrices, four are 100% defect free. From the two matrices with defects, one showed one and the other six defective rows. The defect signature is a significant shift in the threshold voltage (V_{TH}) to more positive voltages and is very likely due to to gate / cleargate defects. As the threshold voltage for the pixels in the defective rows is less positive than the complement gate potential, the defective rows do not affect the measurements of pixels in other rows. It will have to be investigated how these defects influence the dynamic properties of the matrices when operated as detector. Note that in the following discussion, data from failing rows is omitted for the statistical evaluation of transistor parameters.
In general, the devices showed good homogeneity with only a moderate variation in the performance for matrices from different wafers. This allows to exemplarily discuss the transistor characteristics for one matrix in the following paragraph and then to briefly compare the devices in section 4.2.

4.1 Device performance

The first analysis step is the investigation of the pixel's transfer characteristics. A typical dataset for ten pixels is depicted in figure 4(a) on logarithmic and, in the inset, on linear scale. All ten pixels show the expected transistor performance with only small variations from pixel to pixel. The threshold voltage was found to be $V_{TH} \sim 0$ V. In order to compare the properties of all 4096 pixels, the gate voltage necessary to drive certain currents is evaluated for all transistors, and complementarily the transistor current at certain gate voltages. Figure 4(b) shows the projection of the gate voltage V_G at the working point $I = 125$ μA onto the pixel map.

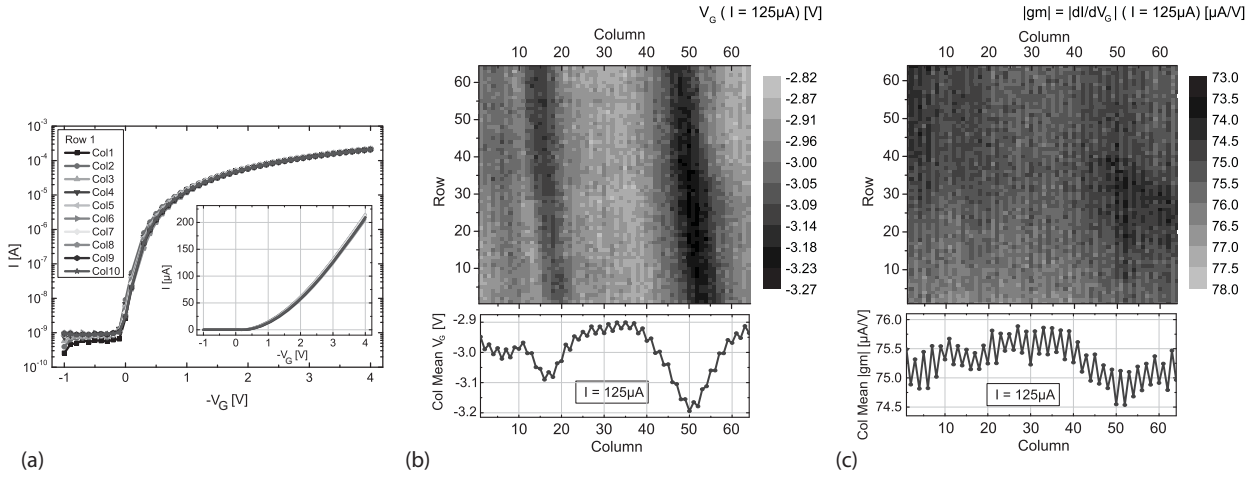

Figure 4. Transfer characteristic. (a) Transistor performance: current versus gate voltage for pixels in the first 10 columns of row 1. The main image shows the data on a log scale, the inset depicts the same data on a linear scale. (b) Map of the gate voltage necessary to force $I = 125$ μA transistor current. Below the column mean of the voltage map is plotted. The even-odd effect and the "dark stripes" effect are clearly visible. (c) Map of the transconductance $\mid gm \mid = \mid dI/dV_G \mid$ at $I = 125$ μA. Below the column mean of the transconductance map is plotted.

The plot reveals a distinct structure in the distribution of the gate voltages. Pixels which are located in the so called "dark stripes" region of columns 17 and 50 require a more negative gate voltage to force the current than other pixels. This prominent effect is also visible in other measurements, see figure 5, and it was found that it propagates over both matrices from the same wafer, as will be shown in section 4.2. The "dark stripes" effect is attributed to a doping variation of the internal gate. The magnitude of the doping variation can be estimated by two methods, on the one hand by the variation in the current distribution of the transfer characteristics and on the other hand from the clear characteristics by evaluating the shift in the clear voltage necessary to provide a complete clear. From both methods it was found that the variation of the deep-n doping of the internal gate is less than $\sim 3\%$ for all matrices. From these results it is obvious that DEPFET pixels are very sensitive to variations of the deep-n doping and therefore the measurement of the pixel characteristics allow to closely monitor the doping homogeneity.

Underneath the voltage map in figure 4(b), the corresponding column wise mean of the voltage is plotted. The dark-stripe effect is evident and also a small superimposed even-odd variation of the gate voltage between neighboring columns is visible. This even-odd effect becomes even more apparent when looking at the transconductance $\mid gm \mid = \mid dI/dV_G \mid$, as depicted in figure 4(c). The even-odd variation is attributed to the specific geometrical boundary conditions for the MIXS pixel during the structuring of the DEPFETs by direct wafer lithography (DWL). Using DWL, the photoresist is structured by a laser system scanning in 200 μm wide stripes parallel to the MIXS columns. As the width of a macropixel is 300 μm, three scanning stripes are necessary to write two pixels. Within a single stripe, the intensity of the laser spot as well as the subpixel position cause small linewidth variations. This leads to a column wise periodicity of 2 DEPFET pixels supposed to cause the observed small even-odd effect. Due to design and orientation of the pixels, the gate length of the transistor is most sensitive to these variations. From the data it was calculated that for all six matrices the gate length variation among neighboring columns $\Delta L/L$ is below 6.5%.

Beside the transfer characteristics, the output characteristics pertains to the standard measurements for the investigation of transistor properties. A typical output characteristics for a DEPFET pixel is shown in figure 5(a) for a set of three gate voltages. As the derivative of the current with respect to the drain voltage is obviously unequal zero at high drain voltages, $\mid g0 \mid = \mid dI/dV_D \mid \neq 0$, also the channel length modulation parameter is unequal zero, $\lambda \neq 0$. The inset of figure 5(a) depicts a current map for $V_D = -2.5$ V, $V_G = -3.3$ V, which reveals the same "dark stripe" and even-odd structure as discussed for the transfer characteristics.

Figure 5(b) contains the DEPFET specific clear characteristics. For the measurement, the clear voltage is ramped down from 10 V to 0 V while the cleargate remains positively biased at 5 V. This allows to investigate at which

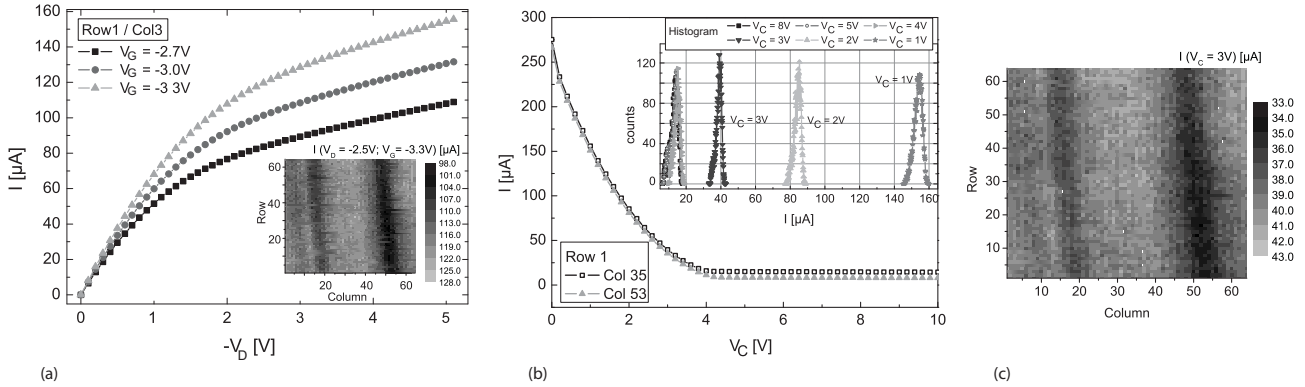

Figure 5. Transistor performance: (a) current versus drain voltage for three gate voltages for the pixel at column 3 / row 1. Inset: Map of the transistor current at $V_D = -2.5$ V, $V_G = -3.3$ V (b) current versus clear voltage for a pixel from column 35 (outside the "dark stripe" region) and column 53 ("dark stripe" region, see map (c)) of row 1. The inset depicts the histogram of the transistor current for various clear voltages. (c) Map of the transistor current for $V_C = 3$ V.

threshold voltage the clear starts to be incomplete, meaning that not all electrons are removed from the internal gate and the remaining charges lead to an increase in the transistor current. The graph depicts data for a pixel which is located in a "dark stripe" and a second pixel outside this region. As expected, for the pixel in the "dark stripe" region the threshold voltage for a complete clear is shifted to somewhat more positive voltages. The inset of figure 5(b) shows the histograms of the transistor current for various clear voltages. A secure complete clear is reached for all pixels at voltages $V_C \geq 5$ V. Anyhow one has to keep in mind that these are DC measurements and that values are expected to shift once the system is dynamically operated as detector. Figure 5(c) contains a map of the transistor current at $V_C = 3$ V, where the transistor current is enhanced due to electrons in the internal gate.

4.2 Device comparison

Comparing the results from all six MIXS devices show good yield and performance of the structures. As already mentioned in section 4.1, the "dark stripe" effect propagates over both matrices from the same wafer, as shown in figure 6(a), where the current maps at $V_G = -3.9$V are plotted for neighboring matrices from wafter 81. This effect is attributed to a variation of the deep-n doping of the internal gate. It was found that the doping variation is less than $\sim 3\%$ for all matrices.
In order to compare the transistor performance of the matrices, the distribution of gate voltages for the working point $I = 125$ μA is plotted for all devices, see figure 6(b), as well as the corresponding transconductance, see figure 6(c). From these histograms the full width of each distribution, $\Delta = \max - \min$, is determined, as this is the key parameter for the design of front-end electronics. The device comparison leads to the following findings:

- Matrices from the same wafer behave similarly. The variation from wafer to wafer is reasonably small. Note that wafers W80 and W81 behave more alike than wafer S81.
- At the working point $I = 125$ μA, the full width of the gate voltage distribution is in the range of 0.44 V$\leq \Delta V_G \leq$ 0.57 V (figure 6(b))
- At the working point $I = 125$ μA, the full width of the transconductance distribution is in the range of 2.80 μA/V $\leq \Delta gm \leq$ 4.83 μA/V (figure 6(c))
- For $V_G = -4$ V, the full width of the current distribution is in the range of 39.1 μA$\leq \Delta I \leq$ 52.3 μA (not shown here).

The full width Δ for these parameters was found to be reasonably narrow, so that the ASTEROID front-end electronics can easily cope with it. The first of the defect free detector matrices is already mounted and operated

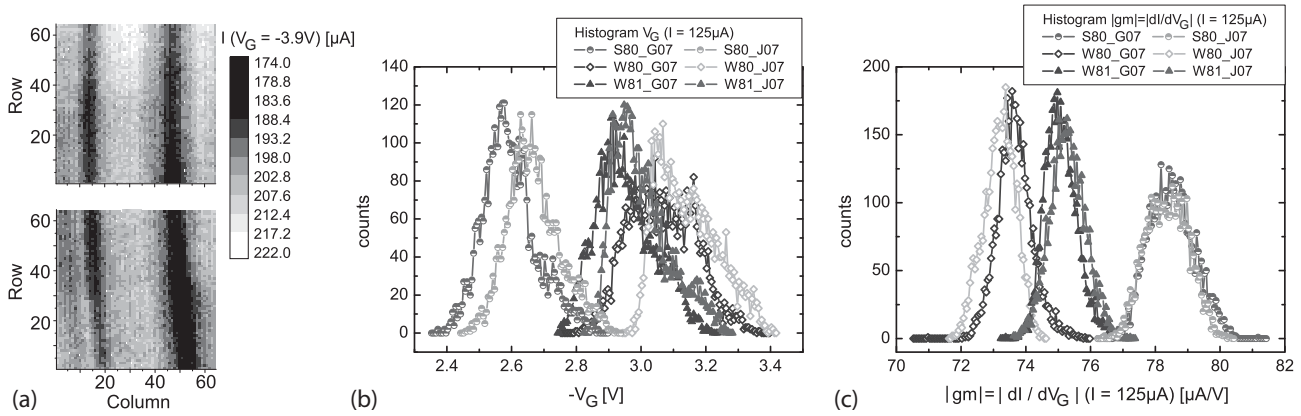

Figure 6. (a) Maps of the transistor current for $V_G = -3.9$V for neighboring devices G07, J07 from wafer W81. It is obvious that the doping characteristic is not a local effect but propagates from one matrix to the next. (b) Histogram of the gate voltage distribution at $I = 125$ μA for all six devices. (c) Histogram of the transconductance distribution at $I = 125$ μA for all six matrices. Devices from the same wafer share the symbol type. S80: semi-filled circles; W80: open diamonds; W81: triangles.

in the electrical configuration which will be used for MIXS. First preliminary measurements showed the excellent imaging capabilities of the system and the spectroscopic performance is currently under investigation.

5. SUMMARY AND OUTLOOK

A new DEPFET test setup was developed in order to be able to identify the best detector matrices prior to the complex and time consuming assembly of a matrix to a detector system. Via electrical qualification measurements at room temperature, the transistor performance of each pixel is investigated, allowing for fast technology and yield learning. It was shown that these measurements are very sensitive, e.g. to doping variations of the internal gate, providing valuable information for process optimization.

Due to the modular concept of the test setup, it can be easily adapted to various DEPFET devices with differing geometry and number of pixels. Currently the setup is used to investigate the performance of MIXS flight devices by measuring transfer, output and the DEPFET specific clear characteristics. Four out of six matrices were found to be 100% defect free with the remaining two matrices showing defective rows. For all matrices the distribution of the total width for key parameters like the transconductance is reasonably narrow and demonstrate good homogeneity.

The next step will be an upgrade of the system in order to facilitate the measurements of IXO WFI Quadrant Prototypes consisting of 512×512 pixels, an increase by a factor of 64 with respect to the MIXS devices.

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