Nuclear Instruments and Methods in Physics Research A 624 (2010) 360–366

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

A fast current readout strategy for the XFEL DePFET detector

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ARTICLE INFO

Available online 19 March 2010

Keywords:
Current readout
XFEL
Trapezoidal weighting function
Time-variant filter

ABSTRACT

In this paper, we propose a novel architecture to implement the current readout of DePFET Active Pixel Sensor (APS) matrices to be used in experiments at the European X-ray Free Electron Laser (XFEL). The circuit performs a fast trapezoidal filtering of the DePFET signal with a very simple architecture based on a Flip Capacitor Filter solution. We discuss the possible available trade-offs between noise and speed performances based on three different timing strategies that can be used to readout the DePFET matrix. Simulation results are shown for a first design of the circuit and expected noise performances are discussed in the last part of the paper.

1. Introduction

DePFET detector is a groundbreaking concept to realize Active Pixel Sensor (APS) matrices for spectroscopy applications and X-ray imaging. This is because DePFETs can provide both detection of incoming photons and amplification of the generated signal [1]. In order to cope with the European X-ray Free Electron Laser (XFEL) [2] experiment requirements, a new type of non-linear DePFET Sensor with Signal Compression (DSSC) is now under study [3]. Two different readout techniques have been developed, a source follower strategy and a current approach.

Due to time constrains – related to the XFEL structure – a dedicated channel must be provided for each pixel detector. The current readout approach has been originally developed in the VELA project [4] on purpose to operate a DePFET matrix at high frame rates, implementing an almost ideal trapezoidal weighing function.

A new architecture to implement the current readout is however necessary to cope with the XFEL requirements, that concern high achievable frame-rate, low noise electronics, area occupancy and power saving. One electronic channel per pixel is needed, as far as switching one channel among several pixels is practically impossible. The pixel size is $200 \times 200\ \mu m^2$ The ASIC will provide one analog filter, an ADC, a RAM and a control logic per channel, and will be bump bonded to the DePFET array; therefore the layout of one pixel channel has to be contained in the detector pixel size. As the final matrix will be 1024×1024 pixels also power dissipation becomes a major issue for the design.

2. Circuit implementation

A possible approach for DePFET matrices readout is based on the source follower configuration, which provides good noise performances, but requires a relatively long settling time when a significant stray capacitance loads the source node. For example, the first integrated circuits designed for DePFETs based on this approach are CAMEX (CMOS Amplifier and MultiplEXer) [5] and ASTEROID [6], with a readout time from 4 to about 16 μs.

To operate at high frame rates, a current readout approach has been already developed and studied for the VLSI Electronic for Astronomy (VELA) project [4]. The VELA ASIC is a 64-multichannel readout chip that overcomes the source follower limitations, thanks to the switched current technique implemented [7], reaching a processing time down to 2 μs/line of the DePFET matrix.

Anyway, even the time required for a single acquisition by the VELA circuit is no longer suitable for the XFEL operation that may require readout cycles down to 200 ns. In fact, the XFEL experiment demands for full parallel readout due to the very short time between subsequent X-ray pulses; therefore, one electronic channel per pixel is needed, as far as switching one channel among several pixels is practically impossible. Moreover, as power consumption and area occupancy become a major issue in the XFEL instrument, the VELA architecture is no longer feasible and other solutions must be developed.

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doi:10.1016/j.nima.2010.03.123

The new flip capacitor filter (FCF) architecture proposed (see Fig. 1) in the paper employs only one operational amplifier to realize the desired trapezoidal weighting function, and also to program the I_{bias} memory cell that subtracts the bias current drawn by the detector in order to have only the signal current processed by the filter.

The DePFET is biased fixing the V_{gs}, as in common source configuration. Since the information is provided on a high impedance node (the drain of the DePFET), the input of the analog chain can be a virtual ground for the signal. A simple cascode stage is introduced before the filter to fix the drain voltage also. This is very important to minimize the impact of the stray capacitance of the DePFET drain on the settling time; in fact, the detector has the source, drain and external gate voltages fixed and therefore – if the cascode was ideal – the stray capacitance would not play any role. This makes it feasible to operate at high frame rates [4].

A programmable current source (see Fig. 2) is set to carry the same current as the bias current of the detector; consequently, the filter receives as input signal only the current variations due to the collected charges in the internal gate of the DePFET. The bias current source must be programmable in order to track the variations of the bias current due to shifts in the threshold voltage of the DePFET after irradiation. A coarse regulation is obtained setting a four-bits digital-to-analog (DAC) converter based on the R-2R ladder configuration, while fine regulation is achieved controlling the gate voltage V_g of the transistors in the activated branches of the DAC.

Acting on these parameters, a bias current from 5 μA up to 150 μA is settable. In XFEL, the X-ray flashes are grouped together in a 600 μs long macro bunch, and macro bunches are separated by almost 100 ms during which no photons need to be detected. This gives the possibility to program the current source before the start of a new macro bunch, and makes feasible to use the same amplifier used for the filtering phase to set the DAC gate voltage when closed in a different loop, once more saving area. One simple inverting stage must be included in the loop to have negative feedback. The fundamental problem related to the current source is that it must have a very low noise, because its noise directly compares with the detector noise, as they both insist on the same node. This forces to use large values for the DAC resistors, above 20 kΩ, and to employ an additional external voltage reference of −3 V.

The sensitivity to threshold shifts after significant dose irradiation [8] is a potential drawback of the current readout solution if compared to the source follower technique. In fact, the source follower is a self-adjusting configuration, as the DePFET changes automatically its source voltage to set the proper V_{gs}, and do not represent any issue. The actual current readout architecture is designed to cope with a maximum threshold shift of 1.5 V. The presence of large non-homogeneities in the threshold shift will be evaluated during the development

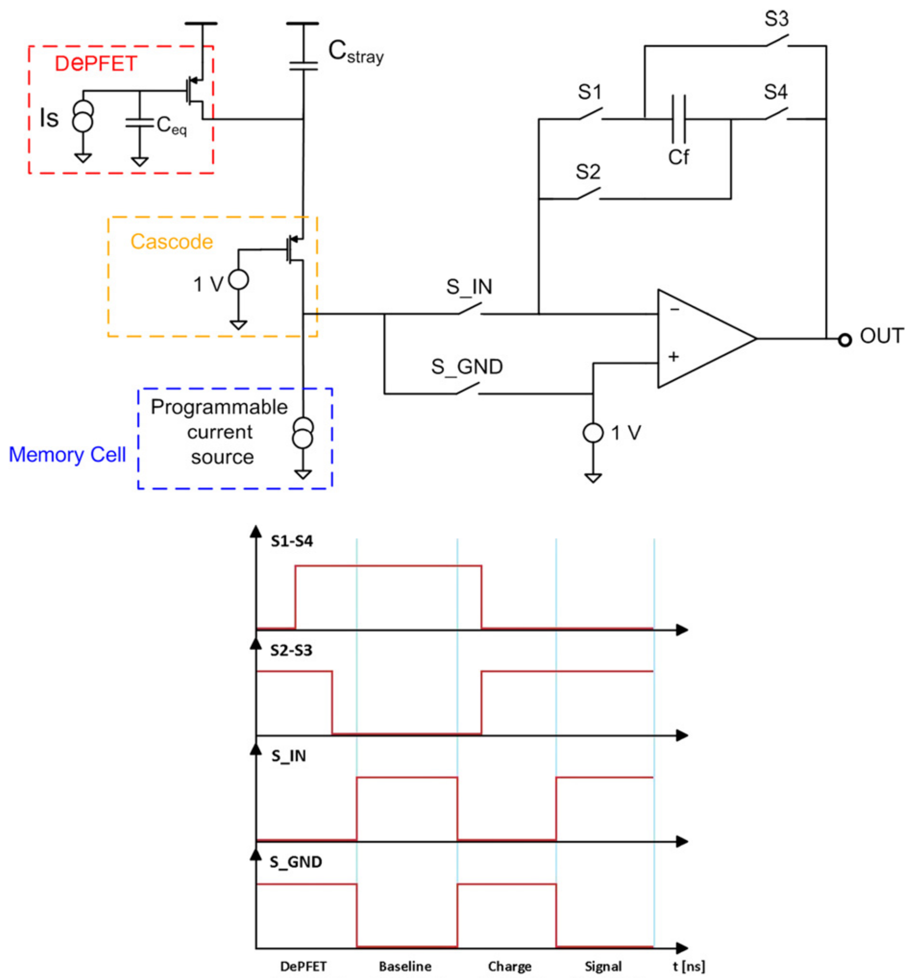

Fig. 1. Schematic representation of Flip Capacitor Filter (FCF) analog filter. In this architecture only one operational amplifier is used, and the desired trapezoidal weighing function is here achieved by flipping the feedback capacitor C_f by mean of four switches [S1 ÷ S4]. The timing diagram of signals controlling the switches is shown.

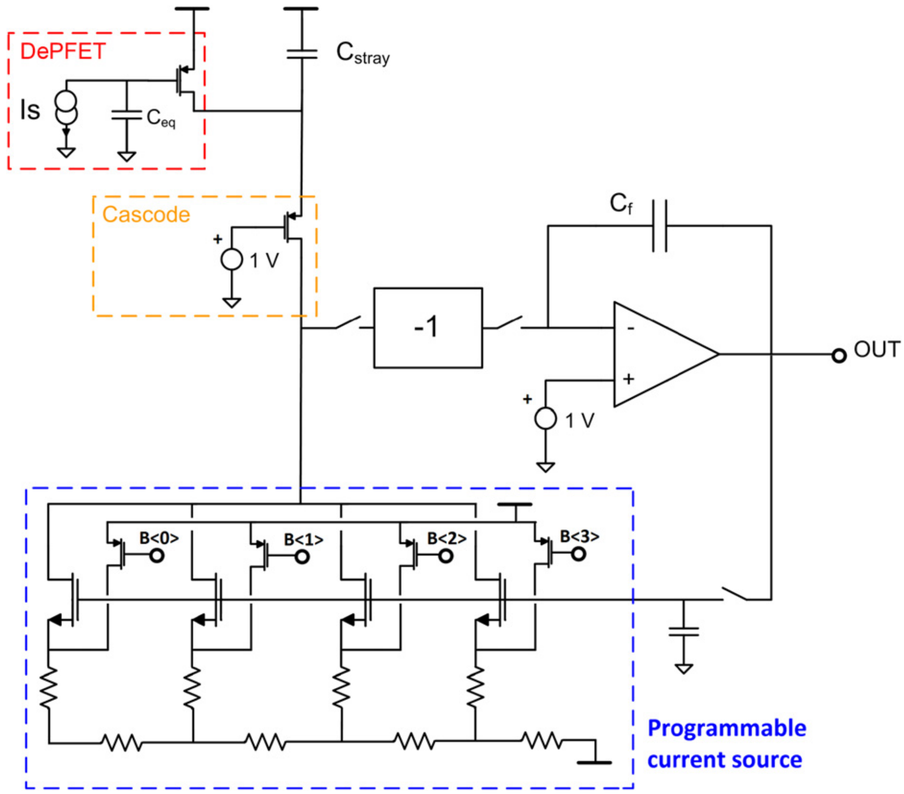

Fig. 2. The programmable current source principle structure. Once the active branches are selected by proper setting of the bits, a fine regulation of the current is obtained working on the gate voltage of these branches. This is done before every macro bunch.

and testing of the new detector and of the absorbed doses in the XFEL experiments.

The signal is integrated by the filtering stage, and the voltage output variation carries the information on the incoming photons. The optimum weighting function to minimize the noise is a triangular one [9]; unfortunately, this result is not achievable due to the collection time of the signal charges needed by the detector that forces the introduction of a finite flattop. Therefore, the aim is to obtain a trapezoidal weighting function that fits in the available period. As already underlined, this is done with only one operational amplifier. The filter uses two correlated measurements to reduce the flicker noise, one measurement of the drain current before the signal arrival (baseline readout) and one afterward (signal and baseline readout). In VELA, this was done by proper switching of the current between capacitors. In the proposed architecture, the desired double measurement is achieved using a single integrator stage and flipping the feedback capacitor C_f by mean of suitable switches. This is the basic idea of the Flip Capacitor Filter (FCF): after a reset interval, a first integration is done to measure the baseline at the input of the filter; then a flattop is present, in which the charges generated by the laser pulse are collected by the DePFET; finally, a last integration is done, measuring both the baseline and the signal, to give the final output voltage. The stray capacitances and the charge injections make the flip phase very delicate. In particular, the stray capacitance C_s that is initially connected to the output node injects a certain amount of charge after the flipping phase; this charge flows through C_f, implying an error in the baseline subtractions. To avoid this problem an additional capacitor C_{add}, is connected in parallel to C_f only during the first integration, requiring an amount of charge equal to the amount that would flow after flipping, thus eliminating this error and preserving the correct amount of charge finally stored in the feedback capacitor after the second integration.

The extremely high energy dynamic range foreseen for XFEL is handled first of all at the detector level, thanks to the DSSC detector. The drain signal current can vary from a minimum of 0.1 μA – corresponding to a single photon at 1 keV hitting the DePFET – to a maximum of 100 μA. To deal with this range, the filter provides a set of four different gains; the desired gain depends on the photon energy of a certain experiment, and is achieved by setting the appropriate number of feedback capacitors in the filter.

3. Timing strategies

The expected time structure of the laser is composed by macro bunches of light pulses separated one from each other by 200 ns. Every group of X-ray flashes lasts for 600 μs, and the spacing between macro bunches is of 99.4 ms. Therefore, when operated at maximum speed, XFEL demands a 5 MHz operation frequency.

It is foreseen that the detector will require about 60 ns both for the clear phase and the flattop phase, during which the generated charges are either eliminated from or collected into the internal gate. Therefore, as a first attempt the 200 ns period can be subdivided into four interval, two of 40 ns and two of 60 ns (see Fig. 3a). A readout cycle starts by clearing the internal gate of the DePFET, to remove the charges of the previous integration (60 ns); then, the baseline is measured (40 ns); the timing of the readout relative to the XFEL structure is arranged such that X-ray pulses arrives after the baseline has been acquired, during what is called the flattop period (60 ns); in the end, a final integration is held measuring both the signal and the baseline (40 ns). Since the feedback capacitor gets flipped during the flattop, the baseline is subtracted and also the flicker noise components are properly filtered by the trapezoidal weighing function implemented.

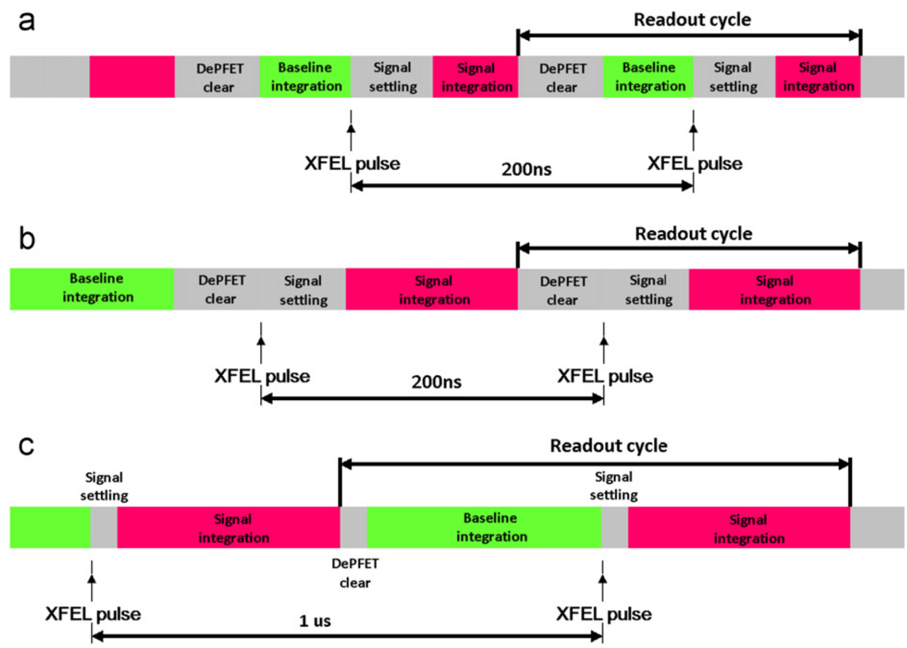

Fig. 3. Different timing strategies for the DePFET matrix readout. (a) Full speed 5 MHz operation sequence timing; every XFEL pulse is detected and the baseline is sampled before every X-ray flash. (b) Timing structure in which a single baseline measurement is done before the macro bunches start; this solution allows more relaxed time constrains for the signal processing, and still every XFEL pulse is detected. (c) If requested by the experiments, the system can also be operated at longer readout times (up to 1 μs).

An alternative solution (see Fig. 3b) would consist in a single baseline measurement before the macro bunch start. Then, in the 200 ns period between pulses, only an integration is held, measuring the signal and the baseline. With this approach, a longer interval – up to 100 ns – can be dedicated for the signal sampling, allowing a reduction of the electronics bandwidth and so a reduction of the white series noise, which is the dominant source of noise at the required speed. It has to be pointed out that in this alternative solution, the flattop of the weighting function gets longer as pulses arrive and consequently the flicker noise is filtered differently for the pulses in the macro bunch, the last one being the more affected; thus, special effort is required to contain this contribution of the front end electronics. The actual contribution of the electronic noise has been estimated and the worsening is totally negligible, even for a flattop lasting for the maximum time of 600 μs.

The possibility to operate the XFEL at a lower speed is also foreseen, suppressing some X-ray pulses and letting just some of them hit the DePFET matrix. In this case, the system can be operated at longer readout times (up to 1 μs) (see Fig. 3c). Anyway, since the drain current provided by the detector is independent from the timing readout scheme, to maintain the same output voltage swing it is necessary to increase the value of the feedback capacitor; if for example a time interval of 400 ns is dedicated to the integrations, it becomes necessary to increase the feedback capacitance in order to maintain the same dynamic range.

All the three readout schemes can be employed by the proposed architecture, simply by changing the timing of the digital signals that control the FCF filter operation.

4. Simulation results

The circuit has been designed in the 130 nm 1.2 V CMOS technology from IBM. Simulations have been performed at the maximum operating speed of 5 MHz and at lower readout frame rates.

Taking into account the subsequent ADC binning of 3.125 mV and that a single photon at 1 keV would generate a current of 100 nA, and since the first photon output voltage should fall in the middle of the first bin of the converter [3], the feedback capacitor in this case must be 1.6 pF. The full range of about 25 μA, corresponding to 8000 photons at 1 keV has been accommodated; in fact, in case of maximum signal with the sized feedback capacitor connected, the output voltage swing is expected to be around 780 mV. The bias output voltage is set as high as 1 V, since the output node has a negative swing.

If more energetic photons, up to 5 keV or more, have to be detected, the gain of the filter can be decreased connecting a suitable number of capacitors in feedback; in the designed circuit a set of four capacitors of 1.6 pF each has been foreseen, for a maximum signal of 100 μA.

The simulations obtained so far very well fulfill the XFEL requirements, and single photon detection is achieved down to the requested energy of 1 keV. In Fig. 4, a typical output voltage waveform is shown, both for minimum and maximum signals; the FCF operation is highlightened. The simulations confirm that the final value of the output voltage after the second integration is independent from the DePFET biasing current, within a simulated range of about 150 μA. In Fig. 5, a detail of the minimum signal output voltage compared to the case of no incoming photons is shown. The variation corresponding to a single photon at 1 keV is adequate to cope with the requirements of the subsequent converter. Since the case of minimum signal is the most affected by offset, Montecarlo simulations have also been done. The filter shows an output variability of 1.8 mV. This is mainly due to two different causes: the first one is the voltage offset of the filter amplifier, attributable to a mismatch in the input stage; the second one is related to different charge injections of the switches, following MOS threshold variations. Although very small, the obtained value is not negligible with respect to the ADC bin amplitude. Thus, a fine offset compensation is still

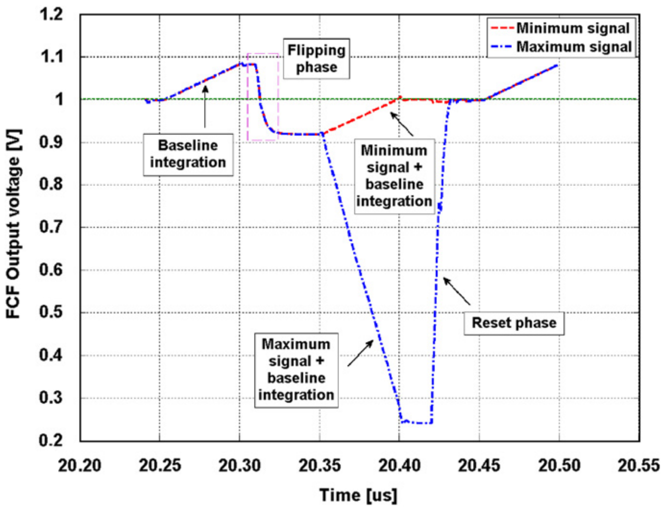

Fig. 4. Output filter voltage swing for minimum and maximum signals at 5 MHz timing operation. Double correlated sampling is simulated with a baseline of −3 μA, and the flipping phase is highlightened.

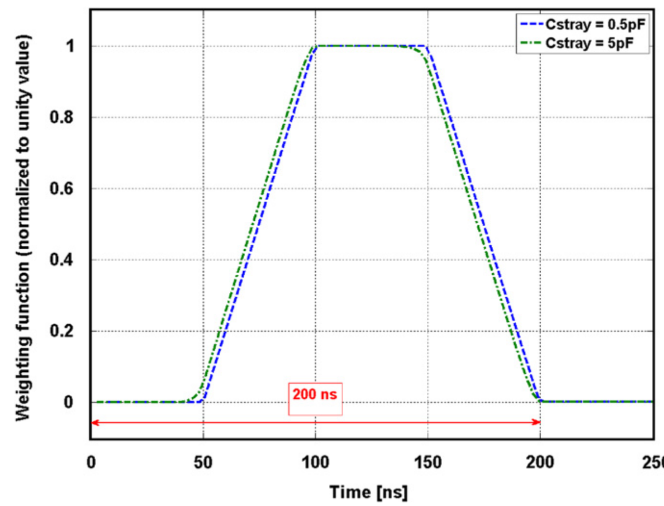

Fig. 6. Simulated weighing function for FCF. Two different stray capacitance values are considered. In both cases, simulations show a well defined trapezoidal behavior. During the central flattop the charges generated by XFEL pulses are collected into the DePFET internal gate.

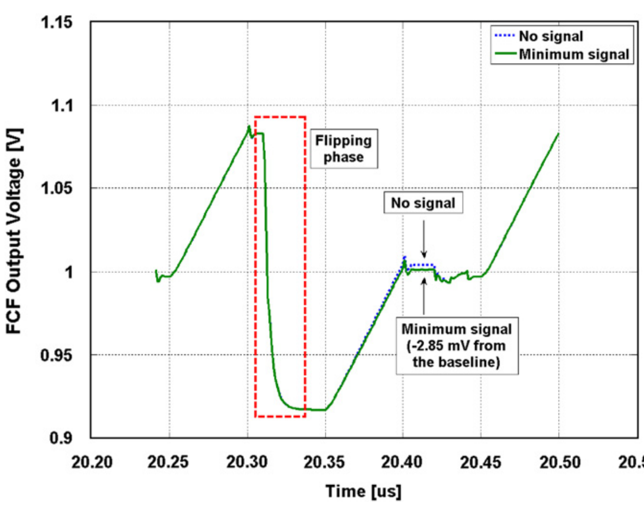

Fig. 5. Comparison between the output voltage without incoming photons and the output voltage corresponding to a single photon at 1 keV. The corresponding voltage variation is 2.85 mV, a value that fulfill well the requirements imposed by the subsequent ADC binning.

needed in order to precisely place the minimum signal average amplitude in the middle of the first ADC bin and to maximize the photon counting accuracy.

Fig. 6 shows the simulated weighing function for the FCF; in this case, the system was operated at 5 MHz. As already mentioned, the trapezoidal weighing function is the better solution to filter adequately the signal. In the figure, two different values of the stray capacitance at the DePFET drain node are considered (0.5 and 5 pF, well beyond the worst expectations). The cascode is not an ideal one and the influence of C_{stray} must be evaluated. In both cases the filter returns an almost ideal trapezoidal weighing function, and so the stray capacitance has a very little influence on the circuit behavior.

5. Expected noise performances

The noise levels achievable with the proposed current readout filter are now evaluated in the complete dynamic range of the input signal. It has to be pointed out that due to the non-linear behavior of the DePFET, the calculation of the Equivalent Noise Charge (ENC) has to be held appropriately.

As already said before, a finite flattop in the trapezoidal weighing function is needed to reset completely the detector; this leads to a trapezoidal weighting function to be implemented. This flattop time reduces the time available for the two integrations done by the filter, for a fixed processing time, thus increasing the series noise of the system. In addition, since the shape of the weighting function is trapezoidal rather than triangular, also the other noise contributions are increased by the flattop time, so this interval must be kept the minimum necessary.

In Table 1, noise performances for a single incident photon are shown, for the three different timing readout strategies discussed. With an operating frequency of 5 MHz, the requirement is that the signal must be read out with an ENC lower than $50e^-_{rms}$ to allow for single photon detection at 1 keV. The simulations done show a total ENC for the system (DePFET and filtering stage) of only $41e^-_{rms}$, thus giving a signal-to-noise ratio of 6.6. The other solutions described above provide better noise performances thanks to the longer time dedicated to the signal and baseline integration phase. As shown in Table 1, the ENC decreases to $27.2e^-_{rms}$ in the single baseline measurement strategy, or even to only $11.6e^-_{rms}$ if the system is operated at 1 MHz. These numbers lead to an expected satisfactory signal-to-noise ratios also for single photon detection down to 500 eV for both the discussed timing strategies.

The above results refer to low energy X-ray photons. When higher energy photons hit the detector, the compressive behavior of the non-linear DePFET must be considered. That is, the gain of the detector is not constant over the dynamic range, and decreases with increasing the energy of the incoming X-ray pulses. Since a given noise contribution at the output of the FCF filter has to be referred to the input of the detector, a worsening of the noise performance is expected at high signal levels. Anyway, in this case the statistical distribution of the number of photons must be taken into account. The statistical distribution is a Poisson one, and therefore the standard deviation increases as the average number of incident photon increases. This means that even if the electronics noise was zero, the measured values of signal would still be affected by the random fluctuations of the incoming photons on the detector; in other words, while single

Table 1
Time parameters vs. expected noise performances for the discussed timing readout strategies. The circuit noise includes contributions from both the filter stage and the programmable current source. Signal-to-noise ratios for incoming photons with an energy of 500 eV are also reported, to underline that it is possible to reach a satisfactory S/N ratio, i.e. larger than 5, even with this energy if using the 1 and the 5 MHz with single baseline measure operation modes.

Readout timing	5 MHz operation			1 MHz operation			5 MHz operation with single baseline measure		
Signal integration	40 ns			400 ns			80 ns		
ENC (electrons)	DePFET	Circuit	Total	DePFET	Circuit	Total	DePFET	Circuit	Total
	$32e^-_{rms}$	$25.3e^-_{rms}$	$42e^-_{rms}$	$10.3e^-_{rms}$	$5.3e^-_{rms}$	$11.6e^-_{rms}$	$22.8e^-_{rms}$	$14.8e^-_{rms}$	$27.2e^-_{rms}$
Signal-to-noise at 1 keV photons	6.7			24			10.2		
Signal-to-noise at 500 eV photons	3.4			12			5.1		

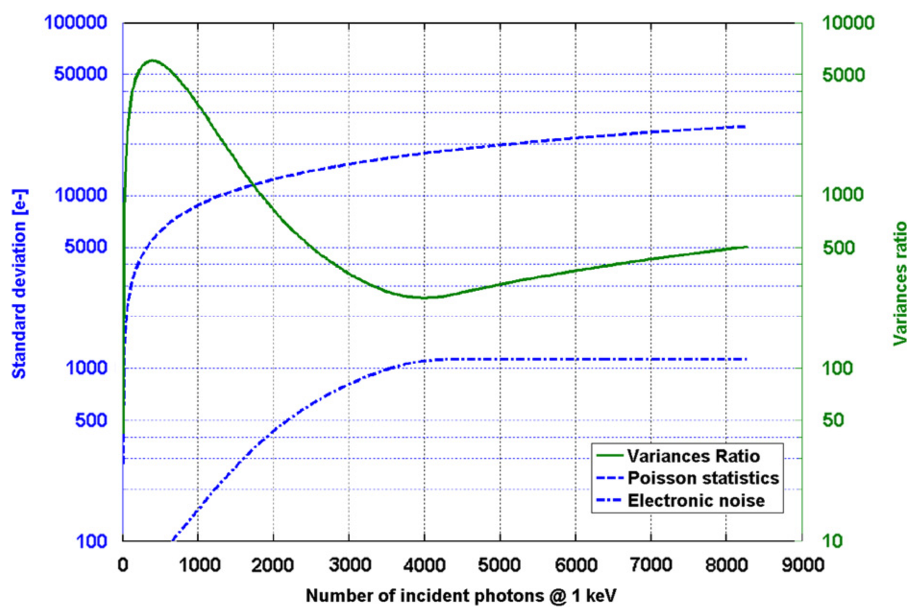

Fig. 7. Standard deviation of the Poisson distribution for the incoming photons and of the electronic noise introduced by the FCF in the whole dynamic range. The ratio of the square of these two parameters is also shown; this ratio increases at higher signal levels and remains greater than unity, and therefore the total noise is always dominated by the photon statistics, even if the electronics noise contribution increases due to the compressive behavior of the DSSC.

photon detection is needed for low signal levels, there is no need to discriminate between 999 and 1000 photons. What is important is that the introduced electronics noise does not become dominant in the front end chain.

This key result is shown in Fig. 7, and it can also be noticed how the ratio between the Poisson's distribution variance and the electronics ENC variance increases at higher signal levels and remains always greater than unity. In any case, it must be clear that the total noise contribution must be calculated as the square root of the sum of the described variances, as it is usual for uncorrelated noise sources.

6. Conclusions

In this paper, we have proposed a new current readout architecture based on the Flip Capacitor Filter idea. This circuit is developed to implement the analog filter in the readout chain for DePFET pixels for the European XFEL. From the simulation results obtained so far, it is possible to operate the system at the maximum required speed of 5 MHz detecting single X-ray photons of 1 keV, with a total noise of $42e^-_{rms}$ dominated by the detector noise itself. Also different timing strategies have been studied, in the case of possible variations in the photons energy according to the experiment requirements, and we have shown that the filter can be easily adapted to cope with single photon detection for energies down to 500 eV. The chip containing the FCF will be submitted soon and tested in the following period to verify the effectiveness of the FCF solution and of the programmable current source.

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